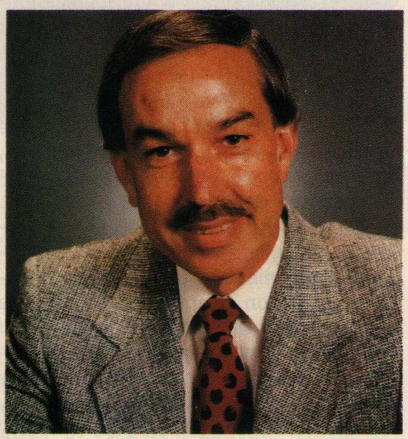
Forecast 1993: Fitting the Pieces Together

Semiconductor International's Editorial Advisory Board shares with you their vision of the industry's future.

Bob Kopp: Device Technology

The technology umbrella for the semiconductor industry looks the same for the next few device generations: it has been shown that we can go to deep-submicron geometries with silicon. I foresee unbroken "Moore's Law" progress in feature size reductions, in die- and wafer-size increases, in component density increases, in reliability improvements and in design innovations, through the 1Gb generation. In all classes of circuits, there will be a freer, more advantageous use of newer, improved components, including bulk-silicon and SOI MOSFETs, floating-gate FETs, and bipolar transistors.



Clearly, for the next several device generations good, effective innovation and development of both process and product are underway in all areas of equipment, materials and device technologies. I believe the rewards will continue to justify and offset the risks.

Most reservations, however, come not from device structures, but from the required tooling, processing and related costs. Issues such as damage control and contamination control present the big technical challenges; many solutions are equipment related. In particular, much of the industry is now focused on the detrimental effects of the process environment seen by product wafers. Particulate and chemical contamination, adverse effects of energetic dry processing and atomic-scale damage all raise major questions about the profitability of future device generations. While control of the wafer processing environment always has been very important to semiconductor technology, the level of concern has increased dramatically as device geometries continue to shrink, increasing the impact of these effects.

Significant particle reductions have resulted from careful interprocess wafer transport through "clean tunnels" and sealed micro environments, such as SMIF pods for which clear, convincing results have been reported only recently. Use of these methods will become widespread.

Process clustering is deservedly receiving a lion's share of attention. Beyond potentially cleaner, higher-yielding processes, integrated processing allows entirely new degrees of surface, interface and contamination controls — process results and devices that simply cannot be achieved otherwise. Besides advanced technological capabilities, the persuasive arguments for integrated sequential processing include lower "cost of ownership" than stand-alone equipment.

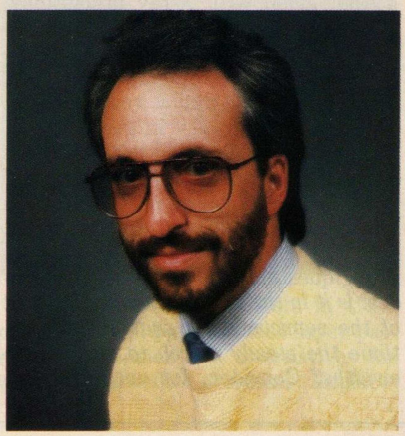
Dr. Robert J. Kopp, Ph.D., PE, *of Kopp Semiconductor Engineering (Albuquerque, N.M.) specializes in semiconductor device technology and its relation to manufacturing, materials and equipment. A consultant for ten years, Kopp previously worked at Fairchild and HP.*

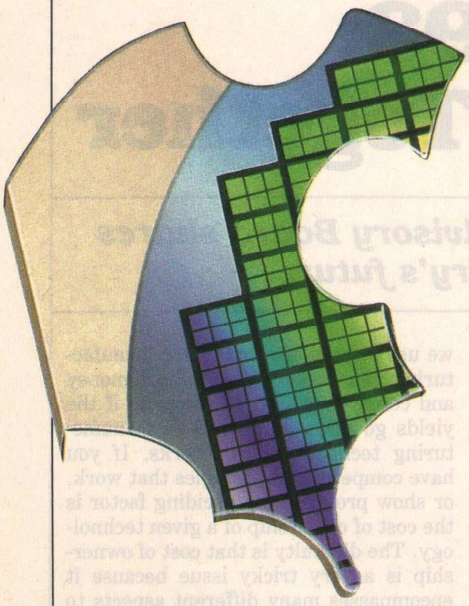
Chris Mack: Lithography

Sometimes we forget that cost-effectiveness determines what technologies we use in each semiconductor manufacturing generation; it's all about money and costs. Your costs go way up if the yields go down, so you need manufacturing technology that works. If you have competing technologies that work, or show promise, the deciding factor is the cost of ownership of a given technology. The difficulty is that cost of ownership is a very tricky issue because it encompasses many different aspects to which researchers don't often pay much attention.

Looking specifically at lithography, cost of ownership issues will continue to push the extension of optical lithography as far as it can go. The transition from i-line to deep-UV will depend in large part on the cost of deep-UV photoresists.

In the long view, it is technically feasible that optical lithography, through deep-UV, is capable of resolutions in the 0.20 to 0.15 μm range. But understand that 0.20 μm optical lithography is going to be very expensive compared to today's lithography. The real question is, will optical lithography continue to be cost-effective, compared to competitive technologies. Right now no one knows when or if the leading non-optical lithography technology contenders, namely proximity and projection X-ray,





will be cost-effective; few in the industry appear ready to make a commitment beyond optical lithography.

Underestimation is a factor that seems to hold back competitive lithography technologies that are potential replacements for i-line. Consider that, while it is maturing now, cost-effective deep-UV resist technology has been difficult, expensive and time consuming to develop.

Phase-shift masking is another technology whose development effort was underestimated: this is a real paradigm shift in the lithography process where we dramatically increase the amount of information on a mask set. Many saw the potential, but failed to estimate the hard work needed to make phase-shift masks work for production applications; we still need to do much work to bring this technology to maturity.

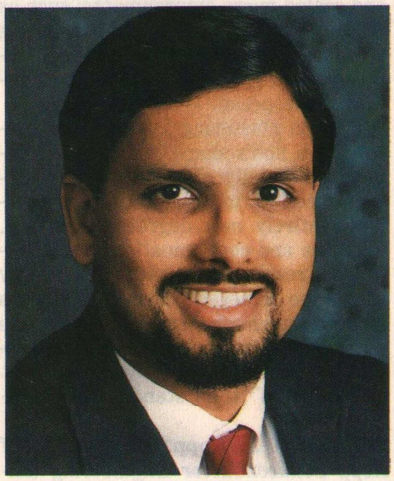
And, again with X-ray lithography, many who first got into this field underestimated the necessary effort. We have learned a tremendous amount from X-ray lithography research that applies to lithography in general, particularly for mask making. But this learning has come at a great expense.

While we will always need to improve lithography technology, at some point out there in the future, there is an overriding question that we all need to ponder: *is it in the best economical interest of the semiconductor industry to continue the steady march to smaller linewidths?* Consider, for example, that memory manufacturers have discovered that with each new device generation they lose more money than they did on the previous generation; profits have been increasingly harder to come by past the 256Kb DRAM. The alternative to relying on smaller minimum feature sizes may be in improving circuit and system design and functionality. □

Chris A. Mack *is vice president of research and development at FINLE Technologies (Austin, Texas): he is the developer of the PROLITH lithography simulation programs. Industry experience includes work at DOD's Microelectronics Research Lab and SEMATECH.*

Venu Menon: Wet Processing

There is still a major role for wet processing: a 0.8-micron CMOS process needs 60 to 70 wet cleans and wet etches. While some are solvent based, these are primarily RCA-clean and HF-based chemistries. Until we have proven more cost-effective alternatives, wet processing is going to be the process of choice.



There is a resilience to wet processing; suppliers seem to engineer it continuously to meet new demands. Recent innovations include cassetteless wet stations, controlled-environment wet benches and single-wafer wet chemistry processors. Of course, we do have equipment reliability and process issues that need continuous improvement.

It is true that we are using some non-wet technologies, but these are typically niche applications. For example, vapor or gas phase cleaning is typically a complimentary "surface prep" process integrated with deposition systems; wet chemistry cleaning is still used before most integrated processes. The only place where I see major inroads by vapor or dry cleaning is before silicide deposition where anhydrous HF processes have proved that they are reliable.

However, the long-term view of most experts is that we have to find alternatives to conventional wet chemistry because of the cost it adds to manufacturing. Wet processing is one of the largest costs in a wafer fabrication facility. Consider that an automated wet bench can cost around $1-1.5 million and a fab equipped for 20,000 wafer starts per month may need 8 to 12 benches. In addition, chemical costs and, particularly, chemical disposal costs have ballooned in the past five years.

Alternatives to conventional wet chemistry are also desirable to provide superior technology solutions to given problems and to make wafer cleaning steps compatible with integrated processing.

A reasonable view is that new uses for vapor and gas phase cleaning will come in critical single-wafer niche applications where they can provide a yield advantage. It is also possible that single wafer wet cleaning could fill such niches. What we should see is gradual adoption of new cleans in these niche applications where either a technical, integration or cost advantage can be developed and demonstrated.

Along with tool and process development, we should also watch the continued development of point-of-use chemical generation. Some published data suggests it may provide an order of magnitude improvement in metallic purity and particle content of typical acids and alkalis. This could give the industry a step function jump in the extendibility of wet chemistry and could also be less costly if chemical generation equipment can be depreciated quickly.

With wet processing research, the overriding theme is that we have not identified a point where it becomes an insurmountable barrier to advanced semiconductor manufacturing. □

Venu B. Menon, Ph.D., *is the contamination-free manufacturing program manager at SEMATECH (Austin,*