Comparison of simulated and experimental CD-limited yield for a submicron *i*-line process

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A method is presented for predicting the critical dimension (CD) distribution and CD-limited yield of a photolithographic process using established lithography modeling tools. The lithography simulator generates a multivariable process response space of final resist CDs versus focus, exposure, maximum resist development rate, and resist thickness. Sources of error are characterized for an actual 0.6-µm *i*-line process. By correlating the input error distribution with the process response space, a final simulated distribution was generated and compared with the actual distribution of the process. Values of CD-limited yield metrics were calculated for the actual process and the simulated data.

Yield modeling for semiconductor manufacturing has traditionally focused on the prediction of defect density to determine a final die yield. Yields have historically been limited by defects. As device dimensions shrink and lithography processes push the design limits of equipment, critical dimension (CD) variations become significantly larger. This increase causes the parameters of manufacturing processes to have a larger impact on yield. As a result, the need to include CD-limited yield is increasing as critical dimensions of lithography decrease.

Accurately predicting a lithography process' CD distribution is possible by using simulation, provided the input parameters for the process and the sources and distribution of errors are known. Once systematic and random errors are identified and characterized, a lithography simulation program can predict the resulting CD distribution. By then assuming threshold values for the upper and lower limit of CDs, this distribution can predict a CD-limited yield to be used to judge the quality of a process.

This paper presents a procedure by which the CD distribution can be predicted. When implemented, the predicted distribution can be used for many purposes. For a new process, the predicted distributions and resulting CD-limited yield provide a metric for gauging robustness. For production processes, this type of study can be used for the optimization of parameter settings as well as identification of critical parameters.

Theory and procedure

The theory of using lithography simulation software to predict CD-limited yield has been discussed previously [1, 2]. This paper focuses on applying the procedure to an actual process. A four-step process for predicting CD-limited yield is shown in Fig. 1. In step 1, error distributions are determined for each input variable of interest in the actual process. In step 2, the lithography simulator [3] generates a multivariable process response space, such as final resist CD versus focus, exposure, and resist thickness. In step 3, a final distribution is generated by correlating the input error distribution with the process response space. In step 4, the output distribution produces a predicted CD-limited yield (or some other metric for the quality of the distribution) using some acceptance criterion for the CD.

In this study, results of the simulated distribution were then compared with the distribution from an actual 0.6-µm *i*-line process. The chosen process, resist patterned on tungsten silicide on polysilicon over an active area, is well characterized with abundant available data.

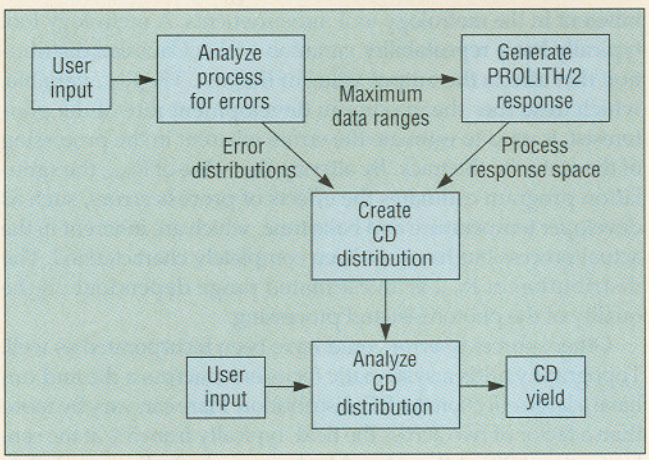

Figure 1: Representation of four-step process for predicting CD yield. User input is required to produce the error distributions from process analysis and to analyze the CD distribution to determine acceptable CD values.

Table 1. Typical sources of process errors

Source of error	Type	Affected modeling parameter
Wafer		
Wafer flatness	Random	Focus
Layer thickness/reflectivity	Random	Layer thickness
Topography	Systematic	Focus
Projection system		
Mask flatness/tilt	Random	Focus
Mask CD errors	Systematic	Mask CD
Exposure repeatability	Random	Dose
Illumination uniformity	Systematic	Dose
Lens heating	Random	Focus
Environmental changes	Random	Focus
Chuck flatness	Systematic	Focus
Autofocus repeatability	Random	Focus
Best focus determination	Systematic/random	Focus
Lens aberrations	Systematic	Focus/aberrations
Flare	Systematic	Flare
Track/resist		
Resist thickness	Random	Resist thickness
Prebake temperature	Random	R_{max}
Prebake time	Random	R_{max}
PEB time	Random	Diffusion length
PEB temperature	Random	Diffusion length
Developer normality	Random	R_{max}
Development time	Random	Develop time
Development temperature	Random	R_{max}
Resist batch variations	Random	R_{max}
Linewidth measurement tool		
Repeatability	Random	Output CD

To simulate the CD distribution of a production process, the sources of process errors must be investigated. Table 1 lists general errors evident in most processes [4], the type of error (random or systematic), and the affected modeling parameter for purposes of simulation. In some cases, an effective modeling parameter can account for the variation in a process input parameter. The error distribution of each parameter must be known. For example, in investigating resist uniformity, the mean and standard deviation of the resist thickness (in the case of normally distributed errors) within the wafer and in wafer-to-wafer samples must be established.

We chose five input variables: focus, exposure, resist thickness, metrology error, and R_{max}. These parameters have a large effect on the CD distribution. The meanings of focus, exposure and resist thickness are self-evident. The metrology error is the variation inherent in the metrology tool measurements. A metrology tool typically has a repeatability variation with a Gaussian distribution that affects the output value of the tool. The R_{max} variable, which describes the maximum development rate of the photoresist, is used to estimate the errors inherent in the processing of the wafer by the track. By altering the value of R_{max}, the simulation program estimates the effects of process errors, such as developer temperature and bake time, which are inherent in the actual process but have not been completely characterized. The distribution of R_{max} is an estimated range dependent on the quality of the photoresist and processing.

Other sources of error could have been incorporated as well. Topography adds a systematic focus error across a die and can have a large effect on the CD distribution. Flare can vary by more than a factor of two across the field, typically from 5% at the center to about 2% at the edge. Mask errors, including mask flatness and mask tilt, can also affect the focus and the resulting resist CD distribution.

Mask CD errors are particularly interesting because their effect may not be obvious. At first, it may seem that the only effect of a mask CD error would be to alter the mean of the resulting resist CDs by the amount of the mask error. The effects of mask CD errors, however, can be magnified on the resist CD [5]. Therefore, the resulting shift in the mean resist CD may be greater than the amount of mask CD error. Also, the mask linearity (resist linewidth vs. mask linewidth) can be nonlinear in the high-resolution region. Consequently, both the mean and distribution of the resulting resist CDs are altered. Although not used in this investigation, this nonlinear effect can be easily included.

To determine the error distribution of each parameter, a random data set was gathered in a testing procedure that analyzed more than 80 wafers. The distribution of each parameter was normal. The testing methodology consisted of a pre-etch measurement of ten points/wafer across five exposure fields. Wafers from 25 lots evenly spaced over a period of two months were selected. Resist thickness measurements were taken on six wafers/day. Of these wafers, two were chosen for E_o (the exposure energy needed to clear the resist from the substrate) measurements. Each E_o measurement had an average of five exposures on a single wafer, and each exposure was in a 1-inch-by-1-inch square. Table 2 lists the resulting distributions.

Obviously, the distributions will be more accurate when more of the error sources listed in Table 1 are included in the simulation. In these experiments, the simulation used fewer sources of error than actually existed in the process. The resulting simulated CD distribution had a lower standard deviation than the actual process.

Several steps were used to translate the distribution data shown in Table 2 into modeling parameters. First, the three distributions for focus data were converted into a single focus distribution by using the sum of squares method for standard deviations. Second, the within-wafer distributions were found to be negligible in relation to the wafer-to-wafer distributions. Consequently, only wafer-to-wafer distributions were considered. Third, the experimentally determined E_o variation was used to determine the proper 3σ values of exposure energy and R_{max} in the simulator. By performing several iterations, 3σ values of exposure energy and R_{max} were found that produced a simulated E_o variation similar to the ±3% seen experimentally. The experimental data for E_o allowed the selection of R_{max} and exposure energy variations that accurately accounted for resist and resist processing errors.

Table 2. Process errors determined for the production process used in this study

Item	Distrib. type	Mean	3σ
Resist uniformity			
Wafer-to-wafer mean thickness	Normal	1.0961 µm	0.03 µm
Within-wafer uniformity	Normal	0.0011 µm	0.00105 µm
Focus			
Wafer flatness	Normal	Nominal	0.3 µm
Focus repeatability	Normal	Nominal	0.2 µm
Chuck flatness	Normal	Nominal	0.075 µm
Dose related			
E_o variation	Normal	115 mJ/cm^2	3%
Illumination uniformity	Normal	Nominal	1.3%
Substrate reflectivity variation	Normal	Nominal	2%
Linewidth measurement tool			
Repeatability	Normal	Nominal	6 nm

Table 3. Modeling parameters used in PROLITH/2

Parameter	Value
Projection system:	
Nominal linewidth	0.60 µm
Pitch	1.20 µm
Wavelength	365 nm
Numerical aperture	0.54
Image reduction ratio	5:1
Partial coherence	0.6
Focal position	–0.5 µm (nominal best focus)
Image model used	High-NA scalar model
Nominal exposure dose	200 mJ/cm²
Substrate	Silicon
Layer 1	Tungsten silicide, 200 nm
Layer 2	Polysilicon, 200 nm
Post-exposure bake:	
PEB time	60 seconds
PEB temperature	120°C
Development:	
Time	65 seconds
Resist system:	
Thickness	1.1 µm
Type	OiR 897-12i

Next, the simulation program created a "process space" of output CDs for many combinations of input parameters. Before calculating the process space, the simulated parameters were "tuned" to match the process [6]. After tuning, the simulator used a "nested multiple run" with inputs of resist thickness, R_{max}, focus and exposure, and an output of CDs. This calculation generated a matrix of combinations containing resist thickness, focus, exposure, R_{max}, and CDs for this process. The simulation parameters are listed in Table 3.

In step 3, the resulting CD distributions are determined from the input error distributions. The probability of occurrence of each combination of resist thickness, R_{max}, focus and exposure was determined based upon the distribution of parameters derived from step 2 (see Table 4) and assigned to the resulting CD. The algorithm altered the resulting CD based on a random number related to the repeatability distribution of the metrology tool. After calculating all probabilities and adjusting the CD for the metrology tool error, the total probability for each range of CDs was compared with the actual distribution data.

Once the simulation distribution outputs are known, it is possible to calculate and compare CD-limited yield metrics. The CD specification must be known to create an upper and lower CD limit. To calculate the yield metric at a nominal ±5% CD specification, for example, the calculated acceptable CDs ranged from 0.57 µm to 0.63 µm. The percentage of total CDs falling within this range can be calculated, resulting in a CD-limited yield metric for that specification.

Table 4. Mean and 3σ values for parameters used in the simulation

Parameter	Mean	3σ
Exposure energy	200 mJ/cm²	6.3 mJ/cm²
Resist thickness	1.10 µm	0.03 µm
Focus	-0.5 µm	0.368 µm
Development R_{max}	160 nm/s	32 nm/s
CD measurement tool error	0	0.006 µm

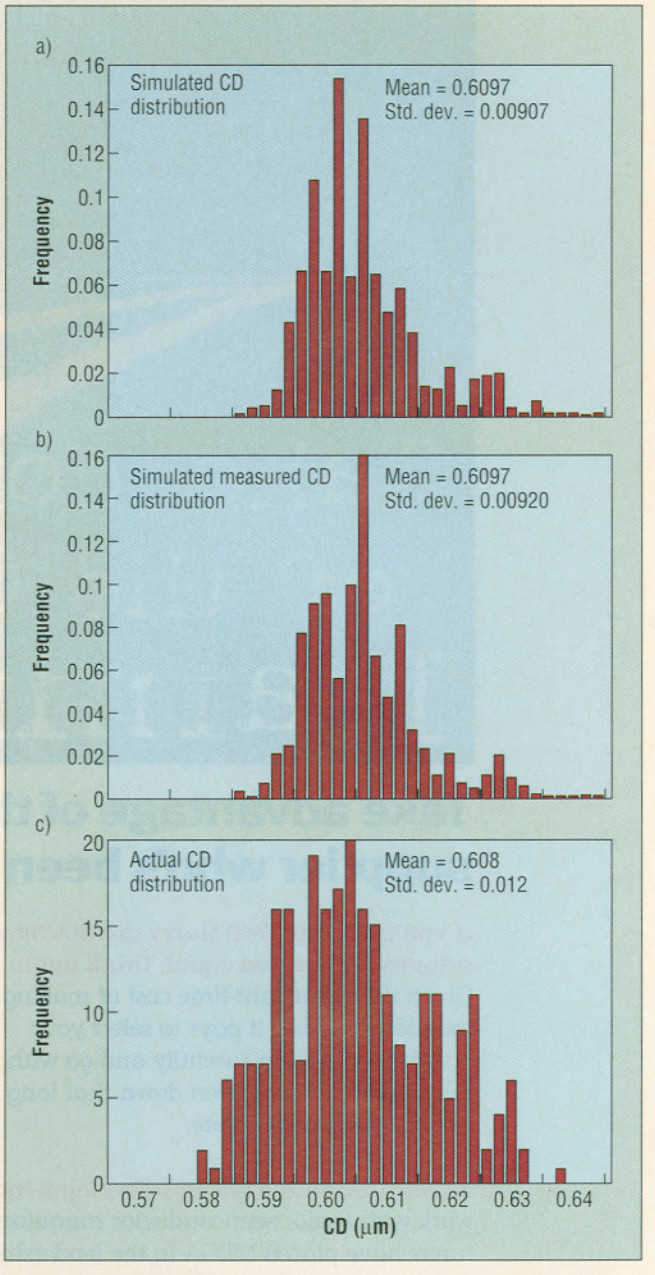

Figure 2: CD distributions for a 0.6-µm *i*-line process: a) simulated by PROLITH/2 showing actual CD; b) simulated by PROLITH/2 including error from the metrology tool; and c) actual data.

Results

The simulated and actual distributions for the process are charted in Fig. 2. The CDs that were predicted to be present on the wafer are shown in Fig. 2a. The simulated distribution after measurement including the error of the metrology tool, and the actual CD distribution for this process derived from historical data are presented in Figs. 2b and 2c, respectively.

The distributions in Fig. 2 are not Gaussian, and have longer tails on the right side than on the left. This skewed distribution is due largely to the variation of resist thickness. Because this process is centered on a valley of the swing curve, any resist thickness variation will cause an increase in the CD. Thus, this non-normal distribution biases the resulting CD distributions.

The simulated distributions (Figs. 2a and 2b) and the actual CD distribution (Fig. 2c) have similar shapes and nearly equal means. The means of a) and b) are 0.6097 µm, and the mean of

c) is 0.608 µm. The simulated distributions, however, have a lower standard deviation than the actual distribution, indicating fewer errors than the actual process. The standard deviation of a) is 9.07 nm, of b) is 9.20 nm, and of c) is 12.0 nm. This result was expected because the simulation took into account fewer errors than occur in the actual process.

The CD-limited yield metrics for four different CD specifications were then calculated for actual and simulated data (for cases with and without the CD metrology error). The resulting yield metrics are shown in Table 5. The simulated yield was consistently higher than the actual calculated yield from the process. This result is expected because the distributions were less scattered for the simulated CDs. If more sources of error were included in the simulation, the resulting simulated yield metrics would more closely match the actual yield metrics. This same phenomenon causes the simulated yield with metrology error to be lower than the simulated yield without the metrology error.

Table 5. CD-limited yield metrics for various specifications of photoresist linewidth

Spec limits	Actual yield metric (Calculated)	Simulated yield metric (Without metrology error)	Simulated yield metric (With metrology error)
Nominal ±5%	95.0%	96.3%	96.0%
Nominal ±4%	86.5%	92.2%	92.0%
Nominal ±3%	76.2%	87.5%	83.7%
Nominal ±2%	65.0%	73.0%	72.1%

In this manufacturing process, the actual yield loss due to CDs that are too large on this gate layer is approximately 3%. Using a nominal ±5% CD specification, the calculated yield metric from the actual data is 95%. There are a number of reasons why the calculated value of CD-limited yield metric is less than the actual observed yield for a process. The distribution used to calculate the yield metric, for example, comprises both die-to-die and within-die values. The yield calculations assume that every CD that is out of specification will result in a failure. A failed die, however, can contain more than one out-of-spec CD, so one would expect the die failure rate to be less than the CD failure rate. Another reason for the discrepancy is that the CD-limited yield metric is derived from measured values. Because the device yield is based on actual rather than measured CDs, the observed yield should be larger than the calculated yield metric.

In practice, the relationship between a simulated CD-distribution and an actual CD-limited yield is very difficult to determine because the relationship between CD and yield is not typically known for a given process. At what CD value does a device fail? What are the CD values that cause performance degradation? Are the failure mechanisms for across-die and die-to-die variations different? These are the types of questions that need to be answered to predict CD-limited yield from a simulated CD distribution accurately. Therefore, it was not the goal of this paper to accurately predict CD-limited yield by using the simulation procedure described. If, however, assumptions are made for the relationship between the CD-limited yield and the CD distribution (as done here by assuming a nominal ±5% CD specification), the resulting yield metric can be used as a comparative value. While this predicted yield may not accurately reflect the actual

CD-limited yield, it can be compared to other yield-metric values calculated in the same fashion.

Conclusion

Several important conclusions can be drawn from this work. First, lithography simulation tools can be used to determine the effects of different types of errors on the CD distribution. These simulation tools can accurately predict this distribution for a process and can therefore be used to characterize a process from the standpoint of CD-limited yield. The procedure for using a software tool to simulate the CD distribution has been developed. The "CD-limited yield metric" that is derived from this procedure can be used to characterize a process, but is only a relative measure of the actual CD-limited yield of the process.

There are several opportune future directions. First, other process parameters can be added to the simulation to produce a different simulated distribution. Investigation of these parameters can determine the sensitivity of the process to each parameter. Second, other outputs can be used. For example, yield could be defined based on a combination of CD, resist sidewall angle, and resist thinning. Third, within-die error can be separated from the total CD error. An investigation of this type would lead to a more accurate calculation of simulated CD-limited yield. Finally, a greater understanding of the physical effects of CD errors on device performance could lead to more accurate CD-limited yield metrics. ■

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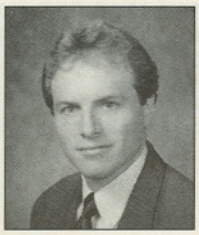

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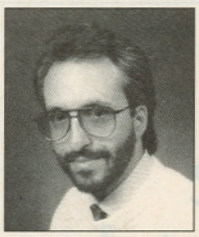

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