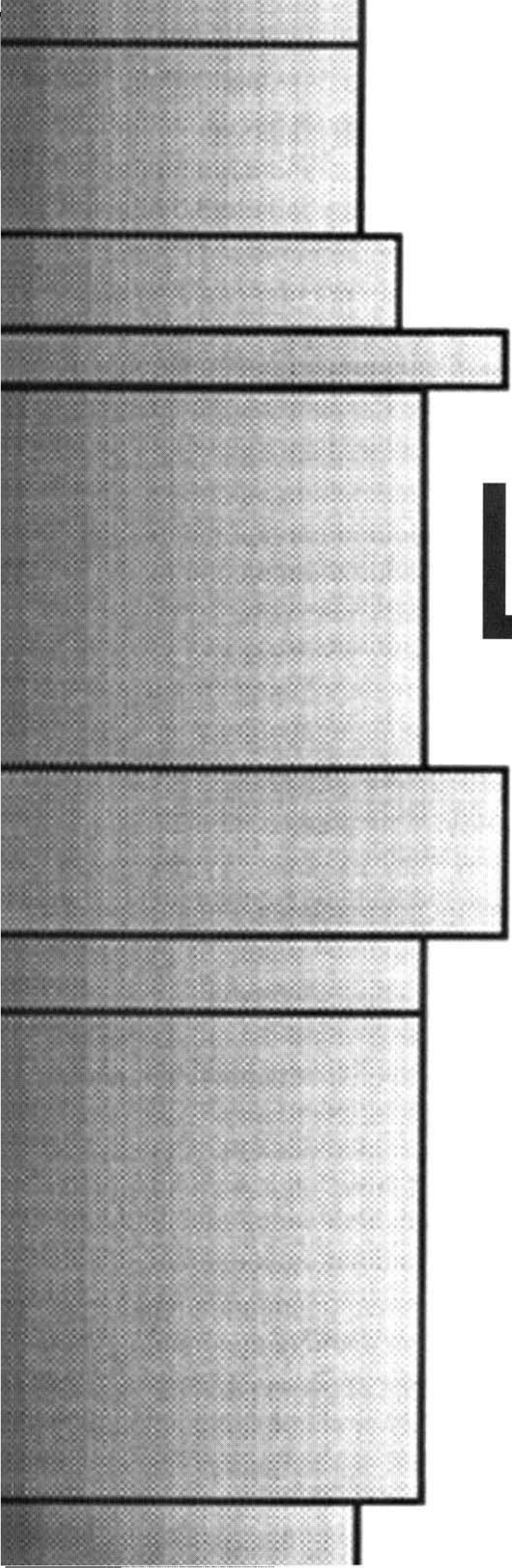

Trends in Optical Lithography

By Chris A. Mack

Snapshot: The author describes optical lithography in the context of the semiconductor industry. Past trends are evaluated and used to predict future possibilities. The economics of the semiconductor industry, and thus optical lithography, is discussed and its impact on technology development explained. Wavefront engineering seems to be the most promising approach to extending the life of optical lithography in the near future.

Optical lithography is the technique for printing ultrasmall patterns onto semiconductor wafers to make the complex circuits that are driving today's information explosion. It is, by far, one of the most demanding applications of classical optical design and fabrication today. Technological advances in optical lithography also deserve a fair amount of credit for the phenomenal growth of the semiconductor industry.

The impact of semiconductor integrated circuits on modern life is hard to overestimate. From computers to communication, entertainment to education, the growth of electronics technology, fueled by advances in

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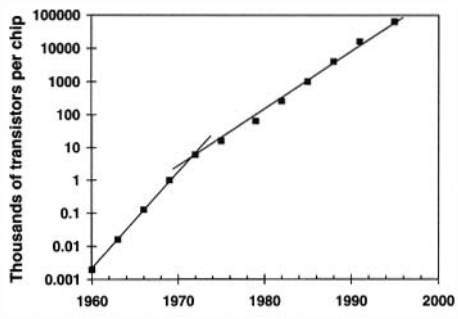

Figure 1. Moore's Law showing an exponential increase in the number of transistors on a semiconductor chip over time (shown here for DRAM initial introduction).

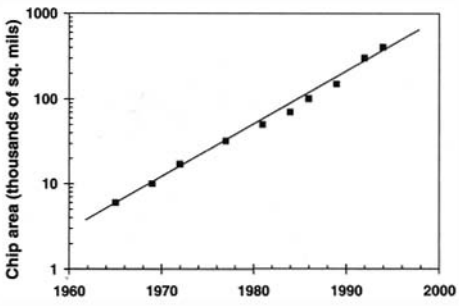

Figure 2a. Moore's Law showing an exponential increase (about 15% per year) in the area of a chip (shown here for DRAM initial introduction).

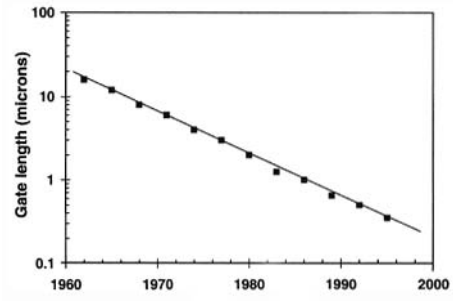

Figure 2b. Moore's Law showing an exponential decrease (about 11% per year) in the minimum feature size on a chip (shown here for DRAM initial introduction).

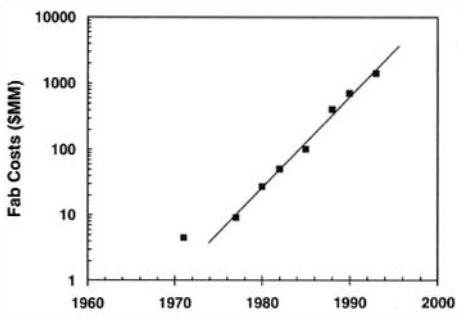

Figure 3. A type of Moore's Law showing an exponential increase (about 35% per year) in the cost of building a new semiconductor fab.

semiconductor chips, has been phenomenal. The impact has been so profound that it is now often taken for granted. Consumers have come to expect increasingly sophisticated electronics products at ever lower prices. The role of optical lithography in these trends has been, and will continue to be, vital.

The remarkable evolution of semiconductor technology from crude single transistors to million-transistor (and soon billion-transistor) microprocessors and memory chips is a fascinating story. One of the first "reviews" of progress in the semiconductor industry was written by Gordon Moore, a founder of Fairchild Semiconductor and Intel, for the 35th anniversary issue of *Electronics* magazine in 1965.[1] After only six years since the introduction of the first commercial planar transistor in 1959, Moore observed an astounding trend—the number of transistors per chip was doubling every year, reaching about 60 transistors in 1965. Extrapolating this trend for a decade, Moore predicted chips with 64,000 transistors would be available by 1975! Although extrapolating any trend by three orders of magnitude can be quite risky, what is now known as Moore's law proved amazingly accurate.

In 1975 Moore updated his law and divided the advances in circuit complexity among its three components: increasing chip area, decreasing feature size, and improved circuit designs.[2] Minimum feature sizes were decreasing by about 11% per year (resulting in transistors that were about 27% smaller in area). Chip area was increasing by about 15% each year. These two factors alone resulted in a 60% increase in the number of transistors per chip each year. Design cleverness made up the rest of the improvement.

That year saw the first (and so far only) change in the slope of Moore's law. In the first 15 years of the semiconductor industry, chip complexity doubled each year. Since 1975, the complexity has been increasing by 60% each year (see Fig. 1). By this time, the design of an individual transistor had reached its optimum—there was no more room for clever tricks to squeeze it further. However, the historical trends for feature size and chip area have continued unchanged (see Figs. 2a and 2b). In an absolutely remarkable achievement of continuous manufacturing improvement, the minimum feature size patterned on a wafer has kept decreasing at a constant relative rate for over 30 years!

After 30 years, extrapolation of Moore's law now seems less risky. In fact, predictions of future industry performance have reached such a level of acceptance that they have been codified in an industry-sanctioned "roadmap" of the future. *The National Technology Roadmap for Semiconductors*[3] was developed by the Semiconductor Industry Association to serve as an industry standard Moore's law. It extrapolates current trends to the year 2010, where 70 nm minimum feature sizes enable 64Gb DRAM chip production (we may need that much memory for future PC operating systems). Compared to today's 350 nm feature sizes, these future lithography requirements will be quite demanding. What imaging scheme will allow the routine, cost-effective production of 70 nm features? It seems unlikely that optics could provide such resolution. Or could it?

The death of optical lithography has been predicted so often by industry pundits, incorrectly so far, that it has become a running joke among lithographers. In 1979 conventional wisdom limited optical lithography to 1 μm resolution and a 1983 demise (to be supplanted by electron-beam imaging systems).[4] By 1985, the estimate was revised to 0.5 μm minimum resolution and a 1993 replacement by x-ray lithography.[5] Today, 0.25 μm production by optical lithography is beginning, 0.18 μm seems likely, and experts hedge their bets on future generations.

Why has optics continued to knock down the resolution barriers? What is the ultimate limit of optical lithography? When will some more advanced imaging scheme with a significantly smaller wavelength (x-rays or particle beams) take over? As with most technologies, the future application of optical lithography will be limited as much by economics as by science.

Economics of lithography

The worldwide market for semiconductor components exceeded $100 billion for the first time last year, and is expected to continue its 20%+ annual growth rate through the rest of the century (some forecasters are predicting a $300 billion market for semiconductors by 2000). Semiconductors both benefit from and fuel

the overall growth in the electronics industry. In 1977 the semiconductor content of electronics products averaged 5%, growing to 10% in 1987 and to greater than 16% in 1994. As a result, the semiconductor market has been growing considerably faster than the electronics market as a whole.

Of course, chip production must grow to keep up with this growing demand. In 1994, the industry produced the equivalent of 52 million 6-inch diameter silicon wafers full of chips. This capacity must continue to rise dramatically to satisfy projected demands. For DRAM production alone, the number of factories (know as fabs in the industry) is growing from 60 in 1995 to over 100 in 1997. Considering that each fab costs well over $1 billion to construct and equip, the result is a significant investment in future capacity. The cost of a state-of-the-art wafer fab has its own Moore's law of sorts, one that is less pleasant to track. Figure 3 shows that new fab costs have grown exponentially over the last 20 years, increasing in cost by 35% each year. New fabs being built this year will cost around $3 billion.

Why does a factory cost so much? Most of the rise in costs is due to increasing costs of the semiconductor equipment used to process the silicon wafers. In 1975, processing equipment comprised 40% of the cost of a new fab. Today, the share is more than 70%. Semiconductor equipment sales have grown from $10 billion in 1992 to $18 billion in 1994, and are expected to be over $40 billion this year. The increasing cost of equipment is to be expected—the equipment is becoming far more sophisticated as the demands of new wafer processes increase. The equipment for lithography is no exception.

Lithography has always been the cost limiter of chip production. The cost of processing a wafer to completion is usually 35–40% lithography costs. The reason is apparent from the fabrication method—each wafer must pass through the lithography process many times to build the complete pattern that makes up the integrated circuit. It seems unlikely that the lithography share of the costs will decrease since increases in circuit complexity result in increases in the number of photolithography steps (called masking levels) that are required. A typical 1Mb DRAM used 11 mask levels, whereas a 64Mb chip requires about 21 masking steps. Furthermore, the cost of lithography equipment is rising faster than the average for semiconductor equipment.

The workhorse of lithography is the optical step-and repeat-camera, known as the stepper. Invented by the now-defunct GCA Corp. in the late 1970s, steppers have kept lock-step with Moore's law for longer than anyone could have imagined. In the process, the cost of a stepper has grown from $500,000 in 1980 to $7 million for today's most expensive models ($4 million is more typical for a state-of-the-art tool today). The cost of a stepper has been doubling every four years (Moore's law at

work again), resulting in no small part from dramatic increases in lens complexity, capability, and quality.

The main imaging lens of a stepper is the most demanding application of commercial lens design and fabrication today. The needs of microlithographic lenses are driving advances in lens design software, spherical and aspherical lens manufacturing, glass production, and lens metrology. There are three competing requirements of lithographic lens performance—higher resolution, larger field size, and improved image quality (lower aberrations). Providing for any two of these requirements is rather straightforward (for example, a microscope objective has high resolution and good image quality but over a very small field). Accomplishing all three means advancing the state-of-the-art in optics. The first stepper in 1978 used an imaging wavelength of 436 nm (the g-line of the mercury spectrum), a lens numerical aperture of 0.28, and a field size of 14 mm diameter. Today's stepper uses a KrF excimer laser at 248 nm, a lens with a numerical aperture of 0.60, and a field size of 35 mm diameter. As you might expect, the cost of the lens has grown somewhat over the years.

Figure 4 shows the growth of stepper lenses, both in size and cost, over the last decade. Lens costs are rising by about 40% each year (compared with the 20% increase in the overall cost of the stepper) and are now in excess

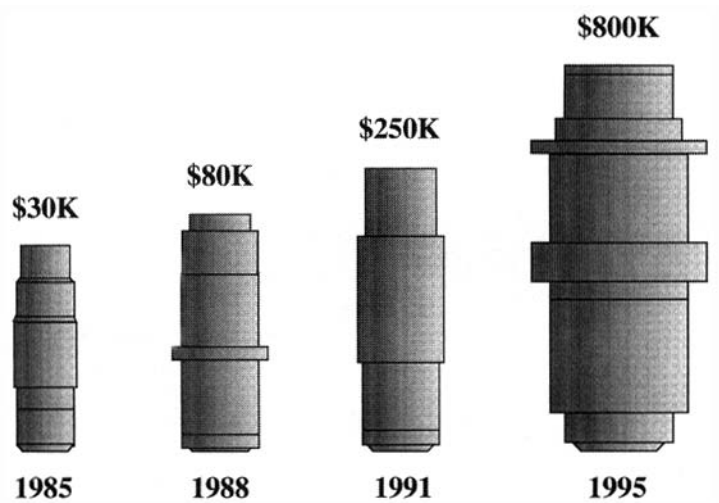

Figure 4. Increase in the cost and size of new microlithographic lenses.

of $1 million per lens. One component of this cost is the raw material itself. Deep ultraviolet lenses require fused silica, costing as much as $10/g (compare this to $1/g for the glass needed for i-line stepper lenses, $0.1/g for camera lens glass, and $0.01/g for plastic needed for a disposable camera lens). Since a 500 Kg lens is roughly 10% glass, the raw material can add $500,000 to the cost of a deep-UV lens before the first surface is ground.

What does this mean for the future of lithography? By the turn of the century, steppers will cost $10 million each. A typical fab, costing $10 billion, will require about 30 steppers to give the 40,000–50,000 wafers/month throughput that will be required. The minimum feature size to be printed will be 200 nm. And in the end, the finished wafers will be manufactured for an overall cost of $4/cm^2 of silicon, the same price it has been for decades. Is this possible? It must be, or the fab of the future will not be profitable. Increases in productivity (through larger wafer sizes and increased equipment throughput) are a necessity. The ultimate goal for lithography is to follow Moore's law of performance at an essentially fixed overall cost.

Technology of lithography

Given the stranger-than-fiction economic environment of semiconductor manufacturing, what technology can satisfy both the cost and performance requirements of a lithography process? So far, only optical projection lithography has demonstrated suitability to the task. Resolution is determined by the wavelength of the imaging light (λ) and the numerical aperture of the projection lens (NA) according to the Rayleigh criterion:

$$R \propto \lambda / NA \qquad (1)$$

One implicit but important assumption is that the image quality is near perfect (meaning very small aberrations) at this resolution. Furthermore, to provide for high throughput from a stepper, the field size of the image must be large. The challenges for improving optical resolution are obvious. Lower wavelengths require expensive, unproven materials (super-pure fused silica and fluoride salts). Higher numerical apertures result in increasing aberrations, which can only be reduced by more complicated designs and more exacting lens manufacturing processes.

To make the situation worse, any improvement in resolution is always accompanied by a decrease in depth of focus (DOF). According to the Rayleigh criterion, the DOF for small features should decrease as the feature size squared. In reality, empirical results have shown the DOF to decrease as about the feature size to slightly more than the first power (as a result of improvements in photoresists and other factors). Still, Moore's law is reducing the DOF by more than a factor of two every six years. Today's 350 nm features typically have a DOF of less than one micron. An important requirement of any improvement in the "practical" resolution of an imaging system is the ability to live within the confines of this reduced DOF.

The difficulties of improving resolution while field size increases and depth of focus remains acceptable has led to a number of innovations that are extending the life of optical lithography. All of today's stepper companies have developed or are developing scanning-based imaging systems to increase the effective field size. Typically, the scanning is coupled with a larger-area stepping motion to accommodate large wafers. The scanning allows a small image field (for example a 25 mm × 2 mm slit) to be used for imaging a large object (say, a 25 mm × 35 mm mask). The smaller field makes the imaging system simpler, though at the expense of more complicated mechanical mask and wafer motion. It is interesting to note that the extension of this concept to the scanning of smaller and smaller areas leads to a raster-scan direct write of the wafer, a notion that has always been rejected for its low throughput. Thus, scanning can be considered as a com-

promise between throughput and lens complexity for large field imaging.

Overcoming the DOF limits is even more challenging. The first approach simply is to live with the tighter focus requirements. Improvements in wafer and mask flatness, autofocusing and autoleveling systems, and wafer planarization by chemical-mechanical polishing of the wafer are examples of how the industry is coping with reduced DOF. In the last 10 years, a second approach has been pursued vigorously by lithography research groups around the world: Is it possible to develop an optical imaging system of some sort that has a combination of improved resolution and improved DOF compared with the classical Fourier optics-based imaging approach?

In general, the optimum image quality for an arbitrary object is obtained by use of a classical imaging system with zero aberrations. Semiconductor lithography, however, uses a very limited set of objects (arrays of lines and spaces, isolated lines, small square holes called contacts, and so on.). In many cases, the sizes of these objects are also limited to set values. Thus, lithography can pose a unique imaging problem—given a single object (say, an array of contact holes of a given size), is it possible to design a special imaging system that is better than a classical imaging system for the printing of this one object? The answer is yes.

The design of an imaging system optimized for a reduced class of objects has been called wavefront engineering by one of the earlier pioneers in this area, Marc Levenson.[6] Wavefront engineering can be thought of in a number of different ways, but essentially it refers to manipulating the optical wavefront exiting the projection lens to produce improved images for certain types of objects. There are three basic ways of modifying the wavefront—manipulating the object (the mask), adjusting the illumination of the object, or modifying the wavefront directly with a pupil filter. The use of a pupil filter (also called apodization) is difficult with current lens designs and is still in the initial research stage. Modified illumination and masks, however, are undergoing rapid development and have even been put into production in some cases.

Typically, a standard imaging system would use an object that is identical to the desired image. However, knowing the limitations of the imaging system, one can design a new object that produces an image more like the desired pattern. By adjusting the transmittance of the mask, one can improve the quality and depth of focus of a given image. Ideally, both the phase and the transmittance of the mask would be modified in whatever way was needed to improve the image. From a practical point of view though, masks for semiconductor lithography are essentially devices with discrete levels of transmittance (the simplest mask is binary, either 100% or 0% transmittance). Each added level of transmittance adds considerably to the cost and complexity of the mask. For this reason, mask modification falls into two categories—mask shaping and phase-shifting masks. Mask shaping uses a standard binary transmittance mask but adjusts the shape of the mask features to improve the shape of the resulting image (for example, by applying serifs to the corners of a rectangular pattern). The difficulty comes in designing the needed mask shapes (remember, a typical chip will require masks with tens of millions of patterns that must be shaped). Phase-shifting masks (PSM) change (or possibly add to) the levels of transmittance on the mask to include phase differences between transmittance levels. Light shifted by 180° will interfere with unshifted light to produced well-controlled dark areas on the image. The difficulty again includes designing the mask, but it also involves more complicated mask fabrication.

Modifying the illumination of the mask will also result in different wavefronts and thus different images. It is well known that tilting the illumination can double the resolution of grating patterns and also can improve the depth of focus of gratings of certain periods. This tilting, however, does not improve the performance of nonrepeating patterns. Thus, the direction (or directions) of the illumination can be customized for given mask features, but there is no one illumination direction that is best for all mask features. (Note that generic imaging applications such as photography use incoherent illumination, that is, illumination from all directions.) Modified illumination (also called off-axis illumination) can be combined with mask modification (either mask shaping or PSM) to produce results better than either approach alone, but with increasingly complicated processes.

Conclusions

The resolution requirements of current and future lithography processes are not so aggressive that they cannot be met with today's technology. Electron beam and x-ray lithography both have demonstrated resolution to spare. The problem is one of cost. Optical lithography is unsurpassed in the cost per pixel (one square unit of minimum resolution) when printing micron-sized and submicron features on semiconductor wafers. To keep the industry on Moore's law into the 21st century, advances in optical lithography must continue. The most promising approach appears to be wavefront engineering—optimizing the imaging system for a small set of important features. There is little doubt that gigabit memory chips and massively complex microprocessors at affordable prices are within reach.

It's still not time to predict the death of optical lithography.

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