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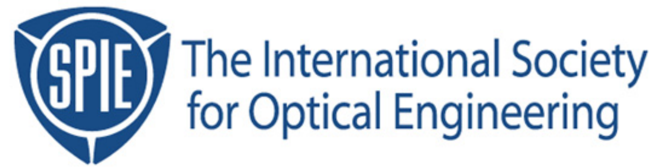

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Phase Phirst! An improved strong-PSM paradigm

Marc D. Levenson[*a], John S. Petersen[b], David G. Gerold[b] and Chris A. Mack[c]

[a]M.D. Levenson Consulting, 19868 Bonnie Ridge Way, Saratoga, CA 95070
[b]Petersen Advanced Lithography, Inc., 8834 N. Capitol of Texas Highway, #304, Austin, TX 78759,
[c]Finle Division, KLA-Tencor, 8834 N. Capitol of Texas Highway, #301, Austin, TX 78759

ABSTRACT

The remaining difficulties in applying dual exposure dark-field strong-PSM technology can be overcome using the Sidewall Chrome Alternating Aperture (SCAA) mask structure, first proposed in 1992[1] and now fabricated. With all silica sidewalls covered and all chrome supported, the SCAA mask is largely immune to the phase and amplitude anomalies that cause space-width alternation as well as the design, fabrication and cleaning difficulties that plague other structures. Maxwell's equation solvers predict that the optical phase will be essentially independent of aperture size. Chips designed with their finest features on a pre-defined regular grid can employ generic SCAA mask substrates in which the topography has been pre-patterned using wafer fab techniques. Guaranteed defect-free SCAA mask substrates will be manufactured in large quantity and low cost if the design grids become standardized. Fabricating strong-PSMs using these Phase Phirst mask substrates will prove no more difficult for mask-makers than COG masks, and the reduced MEEF will permit loosened CD specifications, among other advantages. The Phase Phirst Paradigm promises to reduce optical lithography costs – even for ASIC manufactures – and to delay the need for NGL technologies.

Keywords: Phase-shifting mask, manufacturing, topography, durability, ASIC

1. MOTIVATION

Phase-Shifting Masks (PSMs) get the best possible imaging performance from available optical exposure tools by engineering local destructive interferences. However it has proved difficult and expensive to adapt conventional reticle fabrication techniques to make PSMs – especially strong-PSMs where opposite sides of narrow dark features correspond to opposite phases. While methods now exist to design strong PSMs and the dual-exposure dark-field PSM paradigm is beginning to be adopted in manufacturing, today's strong PSMs are hard to produce in quantity and too expensive for the low volume applications which actually consume the majority of photomasks. In addition, the bare silica trench walls and overhanging chrome cornices characteristic of many designs create imaging anomalies as well as inspection and repair difficulties.

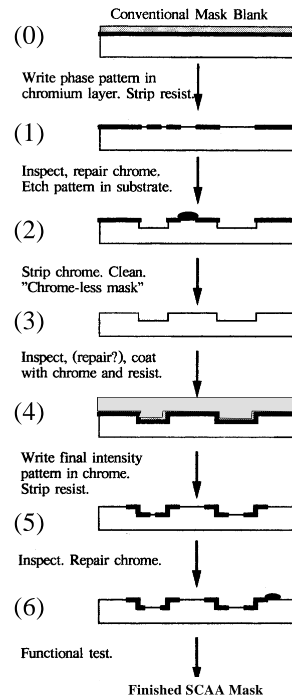

Figure 1. Schematic of a method for fabricating SCAA masks.[1] For reticle-makers, the Phase Phirst process begins at stage (4).

To overcome these problems, one of the authors (MDL) proposed the fabrication sequence shown in figure 1[1]. The end result of this seemingly complex process is a reticle where a film of opaque material conforms to the topography of the phase-shifting layer, which has been fabricated first. This mask structure has been termed the "Sidewall Chrome Alternating Aperture Mask,"

[*] Correspondence: Email: muddle@aol.com, Fax: 408.370.9585, Telephone: 408.370.4837

"SCAA Mask" or "SCAAM."[2] The purpose of this paper is to point out the theoretical imaging and economic advantages of this structure and to demonstrate that it can now be fabricated successfully.

2. FABRICATION CHALLENGES

The first three steps in the production sequence of figure 1 pose no special challenges as they are identical to the production system for "chromeless" masks used for over a decade. The use of a conventional mask blank is only a convenience and less expensive starting material is possible, if it can be assured defect free. Phase errors are minimized by inspecting and repairing the original chrome film, which is treated as a sacrificial hard mask for subsequent dry or wet etch, or a combination of the two. If killer phase defects turn up on the chromeless mask of step 3, that entire substrate can be rejected, re-polished flat and recycled.

Reticle substrate vendors have long known how to coat the opaque chrome layer in step 4 on planar substrates. Figure 2 shows that this same sputtering technology also can coat substrates with topography. The chrome layer on the sidewalls and near the steps of the dry-etched substrate in figure 2a is somewhat thin because of the directional nature of the deposition. Wet etching reduces the wall slope and leads to a more uniform chrome layer as seen in figs 2b and 2c[3]. Chrome films on substrates with topography have defect levels comparable to similar films on planar substrates. The extra cost of this chrome coat step has been one barrier to adoption of the SCAA mask.

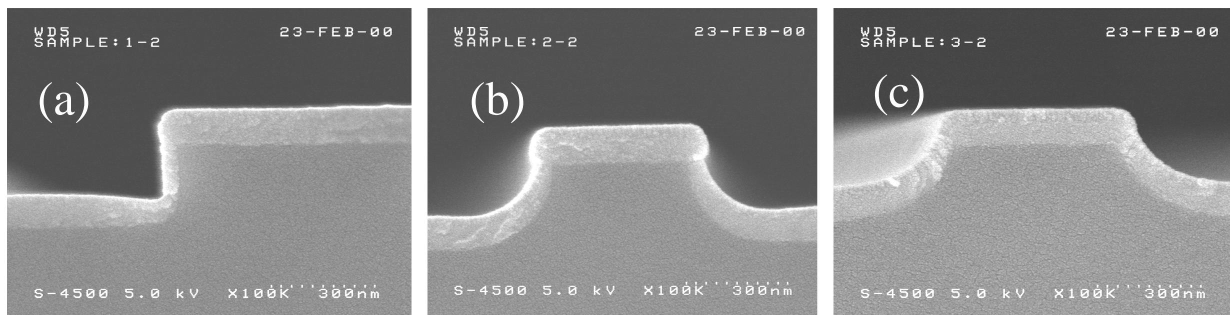

Figure 2. Cross-section SEMs of SCAA mask substrates coated with chrome films in which the phase trenches have been RIE etched (a), wet-etched (b) or dry and wet etched (c).

Once the chrome is in place, a second resist system must be applied as in other alternating aperture-PSM manufacturing schemes. The thickness of this new resist, however, will not be uniform; rather the resist will tend to planarize over the substrate topography, producing a film whose thickness will vary by the phase-trench depth, 244nm for DUV exposure. This variable-thickness resist layer will form the etch barrier for patterning all the apertures in the chrome layer on the final reticle.

The need to pattern a resist layer of variable thickness has been the most serious barrier to fabricating SCAA masks. While wafer fabs have long overcome the many difficulties caused by high substrate topography under planarizing resists,[4] reticle fabs remained fearful of the CD errors induced by resist thickness changes. In fact it proved impossible to pattern a substrate with phase topography using the mask-maker's standard near-zero-contrast e-beam resist – PBS.[2]

Today mask makers are adopting higher contrast resists such as ZEP 7000 for e-beam mask writers and 895i for laser-beam mask writers. Both types produce nearly vertical sidewalls in films <500nm thick, minimizing the effects of resist thickness variation. Optical exposures must, however, continue to cope with swing-curve effects, perhaps by employing TARC and BARC layers or using a planarizing bilayer resist.[4,5] The case of electron beam exposure is somewhat simpler, even at 10keV.

Figure 3 shows the widths of ZEP 7000 lines exposed at 5.94$\mu C/cm^2$ with a 10 KeV beam in resist layers of different thickness as predicted by FINLE Technologies' ProBEAM/3D simulator. A negative 100nm bias has been applied, which has the effect of making the 400nm nominal lines print on-size in 500nm thick resist. The vertical lines indicate the expected resist thicknesses at the 0° and 180° phase levels, which differ by 244nm. Since all critical resist lines straddle these phase steps, the variation in resist thickness has the effect of moving the resist line toward the deeper resist region and increasing the widths of larger features as shown in figure 4a. Thus, for example, for 400nm nominal lines, the resist thickness changes cause both a CD error of 9nm (i.e. a width of 409nm) and a placement error of 76 nm. However, since the phase pattern is in

the mask database, the exposure pattern for the chrome layer can be adjusted to correct for this "proximity effect" by moving the edges in the thick and thin resist as shown in figure 4b in order to compensate for these effects. Figure 4c illustrates how a bilayer e-beam or optical resist process may also ameliorate these shifts by employing a thin imaging layer and transferring the pattern using a dry etch process tuned to produce vertical walls.[6]

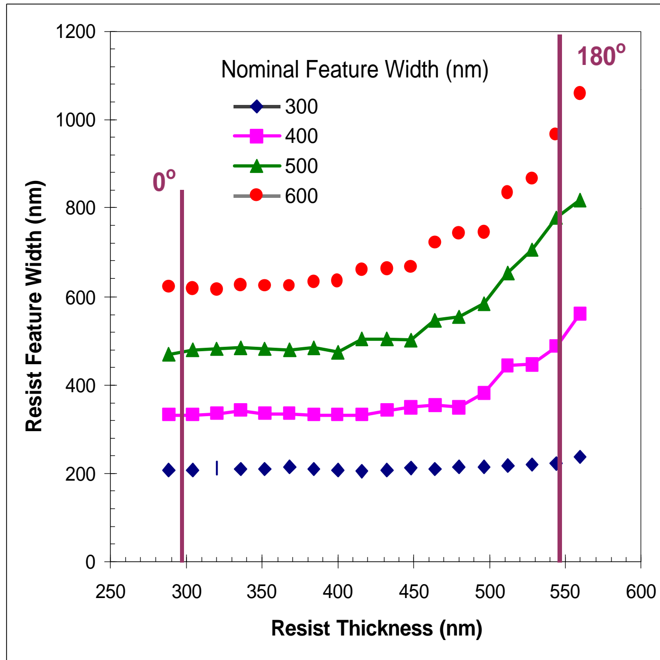

Figure 3. Predicted widths of ZEP 7000 resist lines of various nominal widths as a function of resist thickness when exposed using 10 keV electrons.

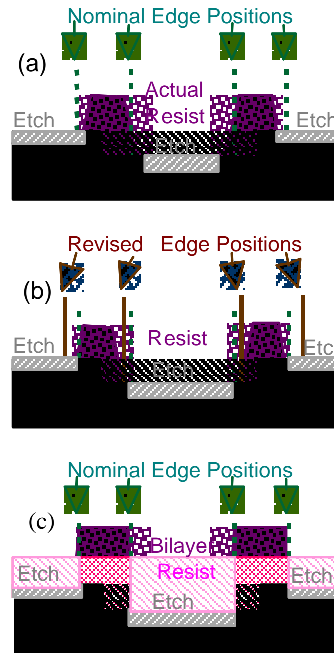

Figure 4. The effect of the thickness dependence of the resist linewidth on SCAA mask structures (a) and methods of correcting this problem by data modification (b) and the use of bilayer resist (c).

The SCAA mask process does not self-align the phase trenches with the chrome features as do processes which excavate those trenches through the apertures in the chrome layer. However, since the phase edges are entirely buried under opaque chrome features that are 4× larger than wafer features and since the chrome apertures which define the exposure pattern are all written at the same time, no great alignment precision is required. For example, if the phase wall is vertical and the chrome thickness is 100nm, the phase step can be anywhere in the middle 150nm of the 400nm wide chrome line needed to define a 100nm gate. It is necessary, however, that the chrome features have correct placement with respect to one another!

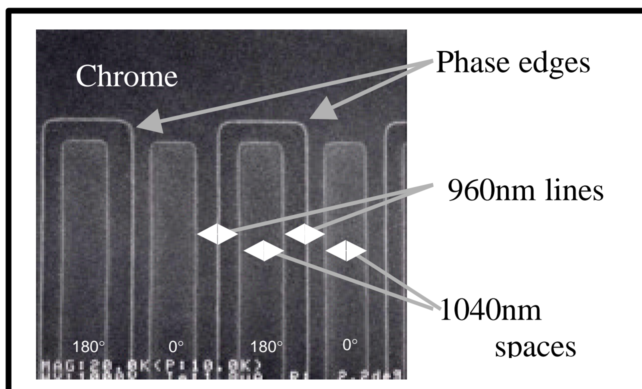

Figure 5. SEM photo of the first successful SCAA mask plate.

Higher energy electrons penetrate further through material than do 10 keV electrons. This greater penetration allows 50 keV electrons (for example) to expose resist films more uniformly, reducing the thickness dependence illustrated in figures 3 and 4. The experimental SCAA mask plate shown in figure 5 was written in ZEP 7000 resist at 50 keV at DNP (Kami-Fukuoka) without extensive data correction for resist thickness variations. Negligible (4.7 ± 7.3 nm) systematic variation between the 180° and 0° spacewidths resulted from residual placement errors due to the varying resist thickness.

The developed resist pattern can be transferred into the chrome layer by standard wet or dry etching and the resist stripped. ICP etching the chrome on the first SCAA mask resulted in a similarly small (-3.3 ± 6.9 nm) difference

between 180° and 0° space CDs as measured at the top of the chrome. Unhappily, this chrome etch process did not produce 90° walls. As the result of sub-optimal wall slopes, the chrome spaces at the quartz substrate varied in width, with the 0° spaces (etched through thin resist on the tops of the phase mesas) systematically smaller than the 180° spaces. Since the spacewidths at the wafer are controlled by the transparent chrome windows at the mask, the images projected by this initial SCAA mask will show a focus-independent spacewidth asymmetry due to this misfabrication phenomenon.

A finished SCAA mask can then be inspected for mouse-bites, pinholes, protrusions and other chrome defects, which can be repaired by standard techniques since all the chrome is supported by the mask substrate. Strong phase-shifting masks tolerate larger linewidth variation (*i.e.* due to repair) than would corresponding COG masks. In addition, the finished mask can be inspected for missing phase shifters and other gross anomalies by confocal, interference and scanning probe microscopy since the surface topography reflects the phase and amplitude structure of the mask. In particular, phase defects at the edges of chrome lines – normally the most dangerous phase defects – can be detected using an atomic force microscope.

The final mask plate would then be cleaned using standard techniques (without fear of particles being trapped in trenches or under overhanging chrome or of removing fine lines), tested, pelliclized and shipped.

3. IMAGING ADVANTAGES

Electromagnetic and imaging simulations of figure 6 show the fundamental advantage of the SCAA mask: Unlike other structures, the immediate environments of the transparent apertures are the same for 0° and 180° spaces. The amplitudes of the 0° and 180° spaces are controlled solely by the sizes of the apertures in the chrome layer and not by surfaces or trenches

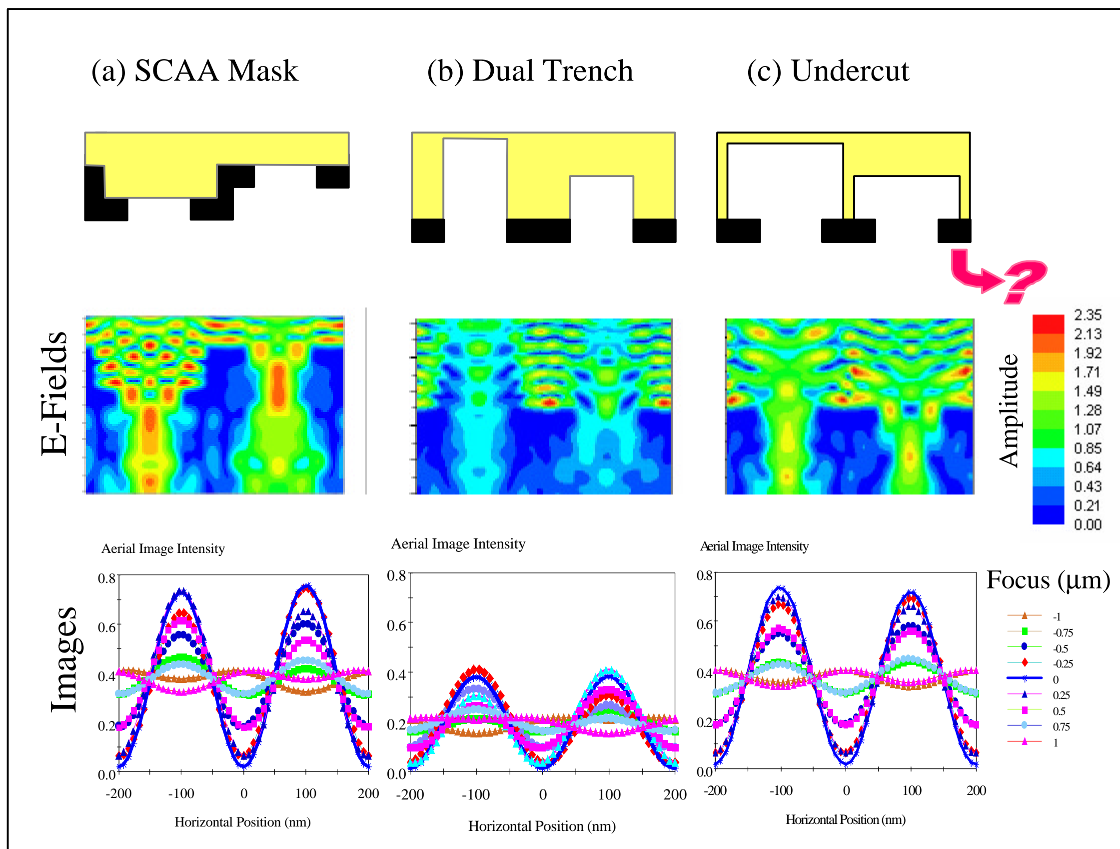

Figure 6. Rigorous electric field simulations at the reticle plane and aerial images through focus for 100nm line – 100 nm space patterns fabricated as a SCAA mask (a), Dual Trench PSM (b) and DPI Undercut PSM (c) as imaged at 248 nm, NA=0.744, 4× and σ =0.2. Image brightness varies more dramatically with space-width in the dual trench design than in other schemes, making it more difficult to overlap process windows. Chrome adhesion can be an issue for the undercut design. These calculations were performed using ProMAX/2D and ProLITH/2 from FINLE Technologies.

above. Thus the electrical field amplitudes for spaces of equal size are the same at the planes of the apertures, which differ only by 244nm (for 248 nm exposure), much less than the depth of focus at the reticle plane of a reduction lens. That means that the SCAA mask images of 0° spaces will be identical to those of 180° spaces at best focus as shown in figure 6a. The phase shift depends only upon the geometrical path length differences. When the phase shifts are not exactly 180°, the images of 0° and 180° spaces differ in brightness away from the plane of best focus as shown in figure 6b. This gives rise to the image-shift effect exploited in the PSM focus monitor reticle.[7] Shifts in spacewidth and line positions with focus are not desired in production reticles. The optical fields produced by a well-fabricated SCAA mask and collected by a projection lens are essentially identical to those of an ideal planar alternating-PSM, avoiding these effects.

The fundamental symmetry between 0° and 180° spaces on a SCAA mask eliminates the need to alter the design to compensate for differing amplitudes and phases (except possibly to accommodate fabrication process biases). There is no need to correct for different transmission factors by biasing 0° and 180° spaces differently or to accommodate non-geometrical phase shifts which depend on trench width and wall surface quality. That is not the case for other PSM structures, such as the single and dual trench designs[8] and the undercut designs popularized by Dupont Photomasks[9] also illustrated in figure 6. To minimize these unwanted effects, the quartz walls in the undercut structure must be etched by >100nm, reducing the robustness of the reticle.

These other designs require detailed mask engineering and OPC just to cope with the non-ideal optical performance, even when the 180° and 0° space transmissions have been made to differ by <5% by biasing the space-widths. Figure 7 compares the space-width dependence of the phase error and absolute transmission as calculated by FINLE Technologies' ProMAX/2D Maxwell's equation solver. The mask geometries in figure 7 have been optimized for 100nm line: 200nm space patterns. In the dual-trench design the brightness of transparent spaces varies dramatically with space-width at the mask plane (figure 7a) requiring extreme OPC just to overlap process windows. Also, the effective optical phases differ as shown in figure 7b even though the geometrical depth remains constant. This effect leads to a reduced common depth of focus.[10] In some cases, the dynamics of the etch plasma can be used to etch phase trenches of different width to different depths (*i.e.* optimized micro-loading). That is not necessary in a SCAA mask process: On a SCAA mask all phase trenches are etched to the same geometrical depth, all (except possibly 100nm) yield ~180° phase shift, independent of width and all have the same transmission. Large-scale etch micro-loading also has less effect since the trenches are always wider than the final spacewidth through which other fabrication schemes must remove substrate material.

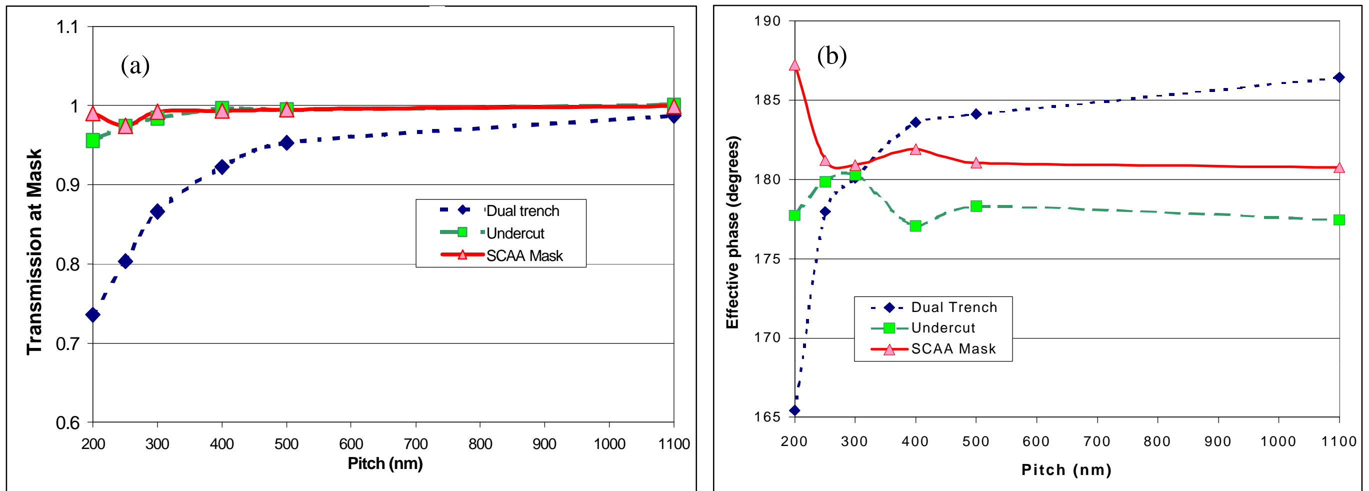

Figure 7. Pitch dependence of absolute transmission (a) and phase error (b) for SCAA, dual trench and undercut PSM designs for 100nm lines. The SCAA mask uses the geometrically-correct trench depth while the Undercut and Dual Trench designs have the phase depth optimized for 300nm pitch (1:2 duty factor). Constant 180° phase shift prevents focus-dependent space-width alternation and image shift.

4. THE PSM PROBLEM

The SCAA masks discussed so far require two pattern writing and two etch steps, as do other alternating-PSMs, and it is reasonable to expect that such reticles would cost more and take longer to make than conventional COG masks. Attenuated-PSMs were expected to require only one write and one etch step, and thus be less expensive to make, but modern tri-tone

designs actually require two writes and etches as well as special blanks.[11] Thus today's PSM manufacturing technologies result in more expensive reticles, often too expensive for many applications. The fragmented nature and low volume of the PSM market has kept mask makers from getting down the learning curve to reliable high-yield PSM manufacturing.

Reticle costs dominate the production expense for chips with 0.25µm and smaller features made in lots of 500 wafers or less[12], but more than half the masks purchased are used for these low volume applications. Since OPC designs and PSMs have been more expensive to make than conventional COG reticles, short-run manufacturers have been hesitant to embrace the advanced optical technologies that have allowed MPU and DRAM manufacturers to reduce gate widths to 100nm or so. The methods developed for the long-production run segment of the industry have been perceived as too expensive, and the ASIC manufacturers have not created their own R&D consortium. The inability of ASIC manufacturers to migrate economically to the deep-sub wavelength lithography regime necessary for gigahertz clock rates has caused some observers to predict the demise of that entire industry segment.[12]

However, the technology and economic environment of the ASIC industry is different from that of the DRAM and MPU manufacturers, where increasing circuit density and reducing die size are the keys to profit. The die sizes of many ASICs are limited by the need for many IO pads. Time-to-market is the key to profitability for ASIC houses. Also, the mask costs so dominate everything else when wafer runs are short that it is good business to reduce reticle costs even if the stepper throughput and number of die per wafer decreases.

These difference in the economic environment motivated one author's (MDL) effort to "reparse the problem" to bring the benefits of two-exposure dark-field strong-PSM imaging to the low-volume ASIC/SOC segment of the semiconductor industry. Such a system would achieve lower costs, higher switching speed and greater die yield but require mask makers to perform only one write and one etch step. If reticle costs were sufficiently reduced, it also might prove acceptable to ASIC houses to compromise design flexibility and circuit density.

5. THE PHASE PHIRST PARADIGM

The key to the Phase Phirst PSM Paradigm is for the mask maker to begin production at step (4) in figure 1, that is with a mask substrate having a pre-patterned phase layer underneath chrome and resist films. The mask maker undertakes only a single write and a single chrome etch as for a conventional COG mask. This simplified process should result in SCAA masks with turn-around times comparable to COG masks and a cost increase related only to the value added by the pre-patterned phase blank. If standard blanks of this sort were manufactured in quantity using wafer fab technologies, Phase-Phirst PSM production might become fast and inexpensive enough to satisfy even low-volume ASIC and SOC manufacturers. Since the ASIC industry is familiar with cell-based design concepts, it may also accept new chip design strategies compatible with pre-patterned PSM blanks.

A chip designed for Phase Phirst production would have all its fine features on sites chosen from a regular grid that is compatible with one of several standard substrate patterns. Larger features – which would not require phase-shift to print properly – could be placed randomly. The PSM in the Phase Phirst paradigm would be mostly opaque, a dark field PSM with windows opened only on opposite sides of narrow dark features. A second exposure using a COG or attenuated PSM would create the connection pattern allowing the chip to function. In the fab, this Phase Phirst Paradigm would resemble the dark-field dual exposure PSM lithography methods that are already being applied.[13,14] Figure 8 shows how the same circuit cell can be made using various phase patterns. The inverse is also true — a single substrate phase pattern can produce many different circuit structures with different chrome openings and blockout masks.

Several different phase patterns would be necessary to address common ASIC designs, but certainly not thousands or tens of thousands. Besides the checkerboard, rectangular checkerboard and island patterns of figure 8, there would also be phase-stripes in both directions and perhaps zigzags and distorted checkerboards with diagonal lines as in figure 9. The x and y pitches of different phase designs would be integral multiples of one another and the smallest pitch would be chosen to allow optimum performance of common exposure tools. For example, a NA=0.62 stepper operating at λ= 248nm and σ=0.3 will print line space PSM patterns with 250nm pitch at full brightness. Thus the smallest Phase Phirst feature might be designed to make that pattern – a 125nm half pitch. At 4X magnification, the substrate features would be 1000nm across, easily fabricated using an *i*-line stepper and oxide-etch technology. The field-stitching problem in making 6" masks using steppers with 22mm exposure fields has already been largely solved.[15] More likely than not, larger pitches would prove more popular for ASICs. The same substrate pattern could be offered with 2µm and 4µm phase trench sizes, fabricated using Canon-style full-field 1X scanners. However, economics would require that each offered phase pattern be applicable to a wide variety of levels and circuits. Otherwise the production runs for each substrate would be too small to amortize the fixed costs of new substrate patterning technology.

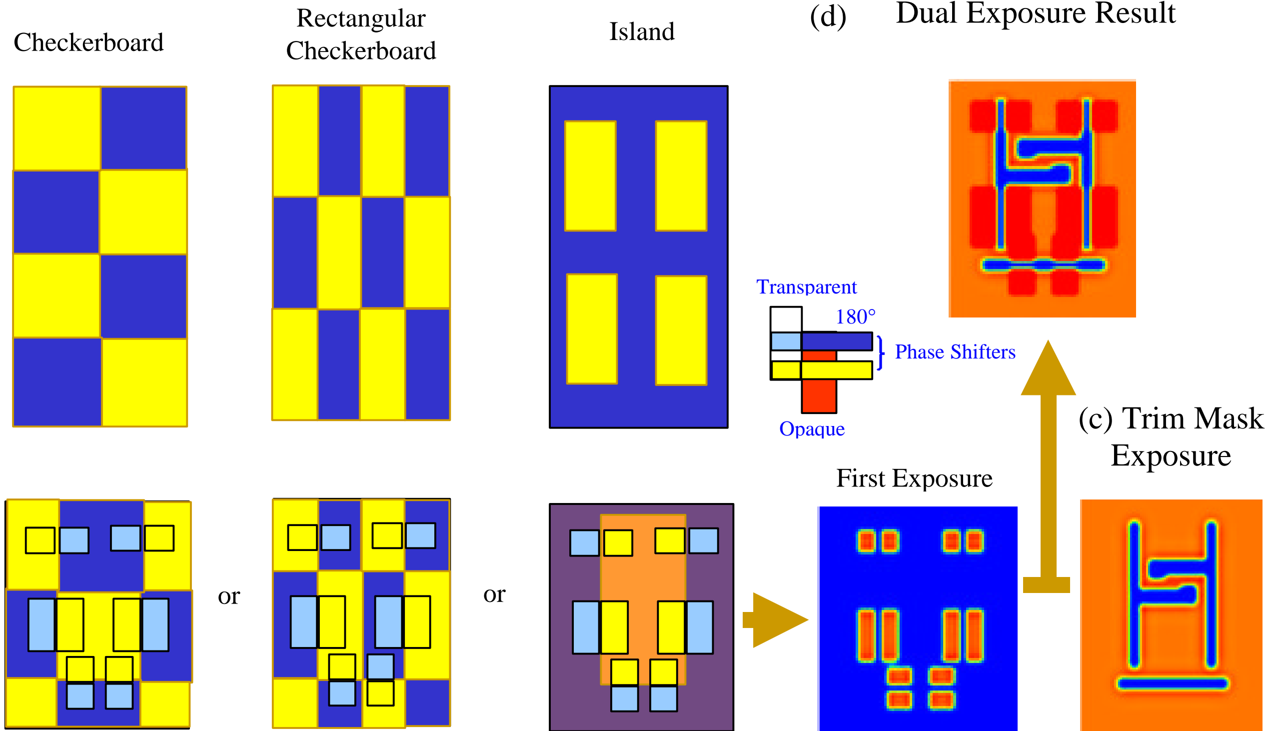

Figure 8. The same circuit cell (d) can be printed using any of several substrate phase patterns (a) with the same transmission windows (b) and trim-mask (c) in the Phase Phirst PSM Paradigm.

Phase Phirst substrate production is a new business, best undertaken by manufacturers of reticle blanks. The optimum process flow appears in figure 10. The Phase Phirst blanks begin as fused silica plates as do conventional COG substrates, but a new high-tech topography creation/inspection process is inserted after the final polishing step and before chrome coating. The proven way to make this topography is to spin on a resist film, pattern it in a stepper using a photomask that defines the phase pattern and then etch the silica substrate to the prescribed depth. Alternatively, a sol-gel or TEOS-CVD silica layer – which etches more rapidly than the substrate – can be applied to the polished surface to improve phase-shift accuracy.[16] The surface topography would then be inspected to insure pattern fidelity and the absence of killer defects. Reject plates would be polished flat and re-used. However, if a substrate was perfect except for a few isolated anomalies, the locations of these phase-defects would be recorded in a database and the plate coated with chrome and resist, inspected and shipped. Since most of the dark-field PSM will remain covered by the opaque film of chrome, it should be possible to use the defect database to match substrate and chip design so that no transparent windows are written in defective areas. Thus the strategy contemplated to make EUV mask substrates affordable will also reduce costs in the Phase Phirst Paradigm.

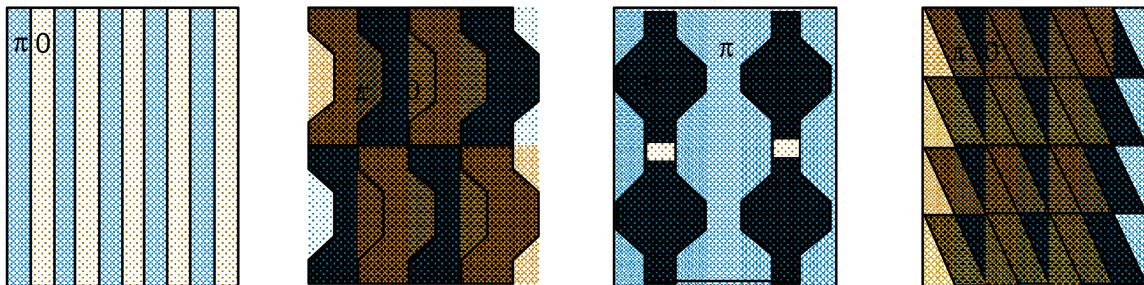

Figure 9. Additional generic phase topography patterns that may prove useful for Phase Phirst.

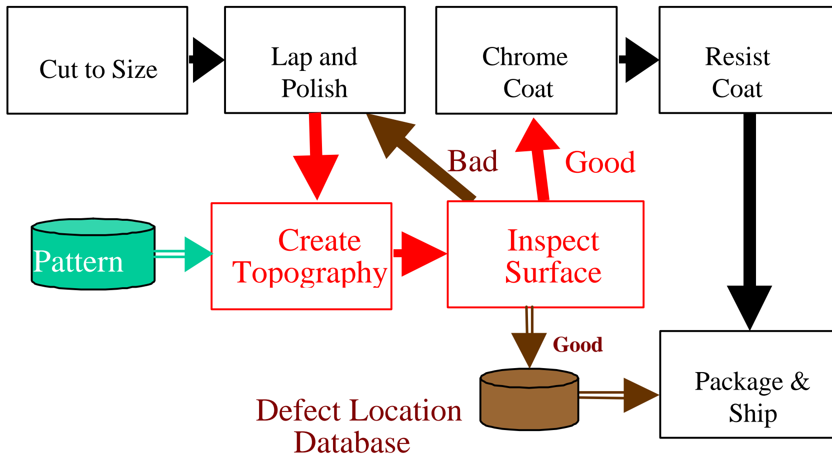

Figure 10. Process flow for fabricating Phase Phirst substrates.

The finished Phase Phirst blanks would be delivered to mask houses where they would be held in inventory according to phase pattern, etc. When a Phase-Phirst job came in, the appropriate plate would be taken from inventory and the chrome apertures written using conventional technology. However, the pattern generator would be equipped to acquire a unique topographic registration mark to assure that the transparent windows were placed properly with respect to the phase edges and the overall circuit. The pattern generator would also write the alignment marks in the chrome layer that would allow the wafer exposure tool to position the image at the proper location on the die. The relationship between the phase-edge pattern and the stepper alignment mark is thus determined by the mask writer during chrome write as in other PSM technologies. Since the phase-shift pattern would already be in inventory, turn around should be three days or less, as for COG plates today. A second trim-mask would be written at the same time to complete the dual exposure dark-field set. Both would be inspected, but since strong-field PSMs have reduced MEEF, CD precision is relaxed, improving yield. The turn around for a Phase-Phirst PSM set for 100nm production should be as fast as for today's 250nm COG reticles.

Unlike other OPC and PSM technologies, Phase-Phirst cannot be implemented by post-processing an existing circuit design. The chip layout must be implemented using EDA software that places the fine features at locations compatible with a pre-determined phase-shift pattern. Most of the required design constraints can be easily implemented in existing systems, and many of today's designs are almost periodic in the sense required by Phase Phirst.[17] The requirement to match circuit features to a phase pattern that is known to lack conflicts considerably simplifies the PSM design process. However, there are likely to be some problems. For one thing the intersections of horizontal and vertical phase edges will require special treatment: On gate levels intersections will have to be avoided, on others, the trim mask will have to be carefully engineered. Also, large transistors used for I-O line drivers will have to be replaced by several transistors in parallel if the required total gate height exceeds the distance between phase intersections on the blank. The overall circuit density is likely to be less than for a design with a fully-customized phase layer, but not dramatically so. The time to first silicon should, however, be dramatically reduced.

6. IMPLEMENTATION BARRIERS

Implementing the Phase Phirst PSM Paradigm requires reticle blank manufacturers, EDA software developers, chip designers, mask makers and wafer fabs to work together. Each will have to compromise with the others. However, most of the profits will go to the device manufacturers, as usual! Coordinating a multifaceted program to validate the Phase Phirst Paradigm in these days of dis-integrated device manufacturing really is the greatest challenge!

However, mask-making economics poses other issues. Roughly 700,000 reticles are made each year, but today <1% are for half pitches <180nm where Phase Phirst would be useful. That is 7000 total masks. If all of them were made on Phase Phirst substrates, the total world-wide demand could be fulfilled by running one stepper at 20 wph for less than 8 hours per week. Unfortunately, there would be little other work for that $7 million tool specially equipped to print 6" square mask substrates! The other tools and processes necessary for Phase Phirst are similar enough to those used in conventional mask-making that they would not necessarily sit idle. However, the CoO of a specialized topography patterning tool and its reticles makes small-pitch Phase Phirst too expensive to implement at a single company with limited (<700/yr) PSM volume requirements. The economics would work best if the Phase Phirst design and production facilities were available to the entire ASIC/SOC industry. Alternatively Phase Phirst substrates with pitch >2µm could be made using a $600,000 remanufactured mask aligner. Such a low-cost substrate patterning system would produce Phase Phirst reticles at costs below strong-PSMs with custom-written phase layers when the volume became larger than about 100 masks per year.

Phase Phirst benefits remarkably from economies of scale. In 2004, Dataquest predicts >80,000 masks will be produced each year for CDs <180nm. If 10% of those employed Phase Phirst substrates, the production cost of those 8000 PSMs would be only ~$2000 more than the corresponding COG masks, rather than 2× or 3× more expensive.[18] The challenge is to capture sufficient volume to make the investment worth-while.

7. CONCLUSIONS

This paper comprised two topics: the Sidewall Chrome Alternating Aperture (SCAA) mask and the Phase Phirst PSM Paradigm. While originally suggested in 1992, the SCAA mask has not yet been developed to its full potential. Regarding the SCAA mask we have:

- Re-introduced the SCAA mask process in which the phase topography is patterned first in the reticle substrate which is subsequently re-coated with chrome and resist for the second write process.
- Shown through electron-beam simulation using FINLE Technologies' ProBEAM/3D and actual experiment that the second write step of a SCAA masks can be performed successfully using ZEP 7000 resist.
- Shown how to estimate the feature placement and linewidth errors due to varying resist thickness and suggested how to correct them through post-processing the data tape, using 50 keV electrons or employing bilayer resists.
- Demonstrated that the chrome can be sputtered onto substrates with topography, covering even vertical walls and sharp corners.
- Rigorously simulated the effects of the mask topography on SCAA mask and other strong-PSM structures using FINLE Technologies' ProMAX/2D Maxwell's equation solver.
- Shown that the potential for phase and amplitude errors due to fabrication and electromagnetic effects are much reduced for the SCAA mask.
- Outlined the defectivity, inspection and repair advantages of the SCAA mask, where all phase steps are covered with chrome and all chrome films are underlayed and supported by the substrate.
- Shown an initial example of a successfully fabricated SCAA mask.

While the SCAA mask does have advantages over other strong-PSM structures, low fabrication cost is not one of them. That problem is solved in the Phase Phirst PSM Paradigm in which:

- IC chips are designed using EDA software that places critical small features at predetermined locations that correspond to phase steps on pre-patterned Phase Phirst substrates.
- Phase-defect free substrates are pre-patterned with a small number of widely useable phase shift arrays using wafer-fab mass production techniques, inspected, coated with chrome and resist and stocked at mask houses.
- Dark-field strong-PSMs and corresponding trim masks are fabricated quickly at mask houses using Phase Phirst substrates for the PSMs,
- Quick turn-around and low mask costs benefit ASIC and SOC fabricators who employ the Phase Phirst PSM Paradigm.

We believe the SCAA mask and Phase Phirst PSM Paradigm provide paths towards widespread insertion of strong PSM imaging, which supports higher resolution and greater process volume than other resolution enhancement technologies. However, the economic advantages of Phase Phirst will not be realized until sufficient production volume appears. When the reticle costs dominate all others and the need for circuit speed requires gates narrower than 180nm, the Phase Phirst PSM Paradigm may be the optimal way to design and build IC's with predicted wafer runs below 500. Experimental demonstration of these advantages is beyond the resources of the proponents of this technology: it requires a joint development program with participants from many different niches. Above all it requires an act of will by some organization.

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