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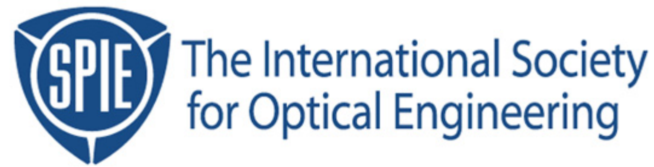

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Measurement and Analysis of Reticle and Wafer Level Contributions to Total CD Variation

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ABSTRACT

The impact of reticle critical dimension (CD) variations on wafer level CD performance has been growing with the trend towards sub-wavelength lithography. Reticle manufacturing, CD specifications and qualification procedures must now take into account the details of the wafer fab exposure and process conditions as well as the mask process. The entire pattern transfer procedure, from design to reticle to wafer to electrical results, must be viewed as a system engineering problem. In this paper we show how hardware and software tools, procedures, and analysis techniques are being developed to support the demanding requirements of the pattern transfer process in the era of 0.13 micron lithography.

Keywords: Critical dimensions, Mask Error Factor, reticle specifications, process window

1. INTRODUCTION

In the not too distant past, reticle critical dimension (CD) qualification was the realm of specialists, those few individuals who understood the arcana of reticle specifications, mask making equipment, procedures and processes, and the unique technical jargon of the mask shop. Mask related conferences were the domain of these specialists, with limited involvement from wafer fab engineers. With few exceptions, most lithography engineers knew little about how an incoming reticle had been qualified. The assumption was that if it had met the specs, it must be a "good" reticle; no further information was required. The reticle was viewed as a consumable, delivered to the fab by external sources just like photoresist, deionized water, and other clean room supplies.

With the ever shrinking CDs on today's reticles and the advent of complex optical extensions such as phase shift masks (PSM) and optical proximity correction (OPC), reticle related issues are becoming an increasing part of wafer level CD control. More and more lithographers are actively investigating the role of reticle CD variations in the final wafer CD distribution.

CD control is now so tight that no one can afford to overlook the critical role of reticle CD variation in establishing viable wafer level CD error budgets. The dreaded Mask Error Factor[1] (MEF), also called the Mask Error Enhancement Factor (MEEF), means that reticle CD errors do not transfer linearly to the wafer level. The lithography process involves a complex transfer function from reticle to wafer. The details of this transfer function must be understood for each type of reticle feature printed. OPC and PSMs add another level of complexity as they add critical interaction terms between reticle and wafer patterns. Only by addressing the entire pattern transfer process at a systems engineering level can users establish workable error budgets, wafer and reticle specifications and inspection strategies, and process control limits[2].

2. THE IMPACT OF MEF

With the total allowed wafer CD variation now in the 10-30 nm range, every nanometer of allowed variation must be carefully assigned in the error budget. Allowing for excessive variation in one component could impose unachievable targets for other elements of the budget. The development of viable CD error budgets requires a detailed analysis of the sources of variation[3] (SoV) and their impact on the final CD distribution. Effectively decomposing the sources of CD error requires separating reticle CD variations from the wafer level CD distribution. This separation is not simply a matter of subtraction due to the complexities of the Mask Error Factor.

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The concept of the MEF has been discussed extensively in the literature[4,5,6]. The MEF can be defined quite simply as the ratio of the change in resist feature width to the change in mask feature width assuming everything else in the process remains constant. In mathematical terms,

$$MEF = \frac{\partial CD_{resist}}{\partial CD_{mask}} \tag{1}$$

where the mask CD is in wafer dimensions (that is, already scaled by the magnification of the imaging tool). An MEF of 1.0 is the definition of a linear imaging result. Although an MEF less than one can have some desirable consequences for specific features, in general an MEF of 1.0 is best.

The term Mask Error Factor is actually a gross oversimplification; it is not a multiplicative factor at all, but rather a complex function of the specific feature type and size. In addition, the MEF for a given feature and mask error varies strongly as a function of process conditions, especially focus errors. The further the process drifts from the ideal focus position, the worse the MEF becomes. The MEF is thus a useful concept for studying process variations, but when it comes to setting reticle specifications what really matters is not the MEF but rather the maximum allowable CD error that a given process can tolerate. <u>It is important to characterize the MEF for all feature types and sizes, and under a reasonable range of process conditions, in order to properly specify the allowed range of reticle CD errors</u>.

Lithography simulation (in this case, using PROLITH/2 v6) can be useful for understanding the complexities of the MEF. All of the simulations in this paper are of 180 nm lines, with the pitch varying from 360 nm (dense line/space pairs) to 420 nm (1:1.5 line space pairs), as well as isolated 180 nm lines. The exposure system is a 0.65 NA 248 nm stepper with a partial coherence of 0.65, and we use a resist model which duplicates the performance of Shipley UV-6 positive tone acid catalyzed resist; the model has not been tuned to match real resist data. The reticles are all chrome on glass binary masks with no subresolution assist features. The MEF is calculated from the ratio of the wafer CD vs. reticle CD curves at the desired reticle bias. Thus, we can speak of the “MEF at zero bias” as the expected wafer level error per nm of reticle level error centered around the point where the reticle has zero error (Fig. 1).

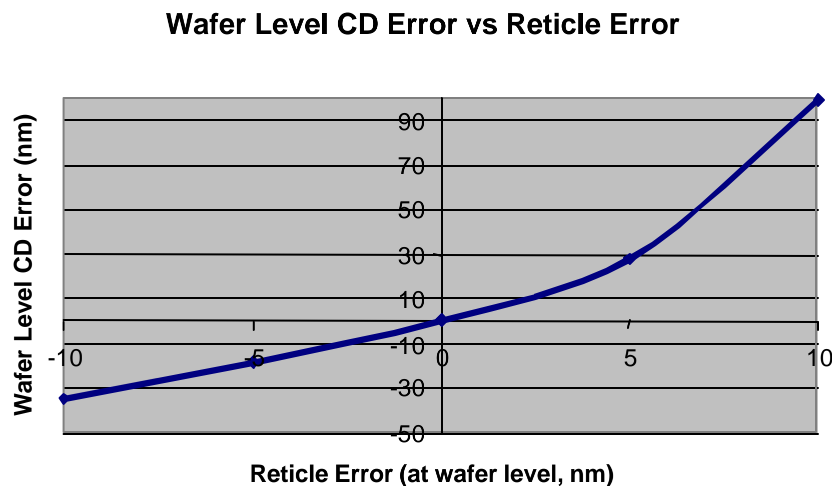

Figure 1: Typical MEF curve showing wafer level CD error vs. reticle level CD error, expressed in wafer level values (dividing reticle errors by the stepper magnification). The MEF for a given bias (reticle error) is the ratio of y to x values at that particular point on the curve.

Consider the linearity curves shown in Figure 2. It should be emphasized that linearity is related to, but not the same as, the MEF. Linearity is the change in wafer level CD vs. reticle CD <u>at a fixed duty cycle</u> (line/space ratio), while allowing the pitch to change. MEF, on the other hand, is the change in wafer CD vs. reticle CD <u>at a fixed pitch</u> as the duty cycle changes. Both MEF and linearity reflect the subtle changes in the aerial images and the interaction of the aerial image with the resist as the process nears the resolution limit of the imaging system. Fig. 2 shows that while isolated lines continue to be resolved fairly linearly down to 160 nm, the dense line/space pairs suffer severe CD non-linearity beginning at 190 nm. As the spaces

become too small, the linewidth grows sharply until the spaces fail to resolve. For this reason, the MEF for a positive mask bias (linewidth on the mask printed larger than intended) will become catastrophically large, as it prevents the space from printing. The MEF for negative bias (chrome lines on the mask printed narrower than intended) can actually be smaller than for zero bias, at least for dense patterns, since it improves the printability of the narrow spaces. This result is shown in Fig. 3, where we show the MEF vs. mask bias for both dense lines and spaces and isolated lines. Note that all of these simulations are performed at best focus and exposure.

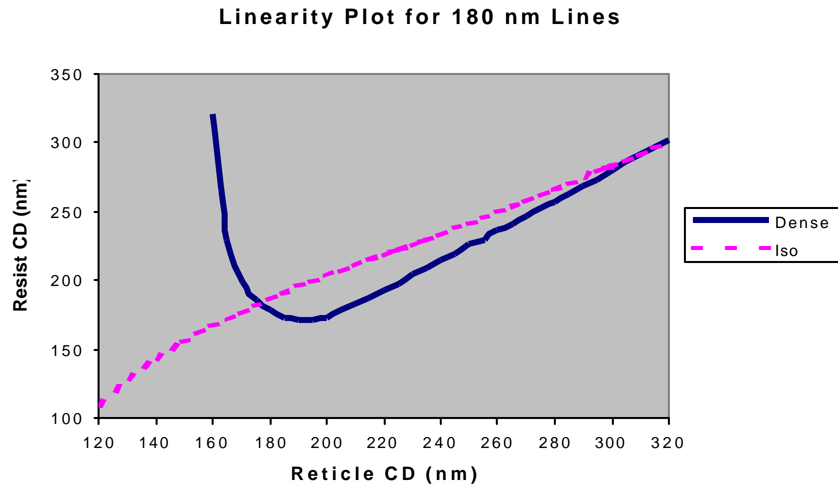

Figure 2: Typical linearity plot for isolated lines and dense line/space pairs.

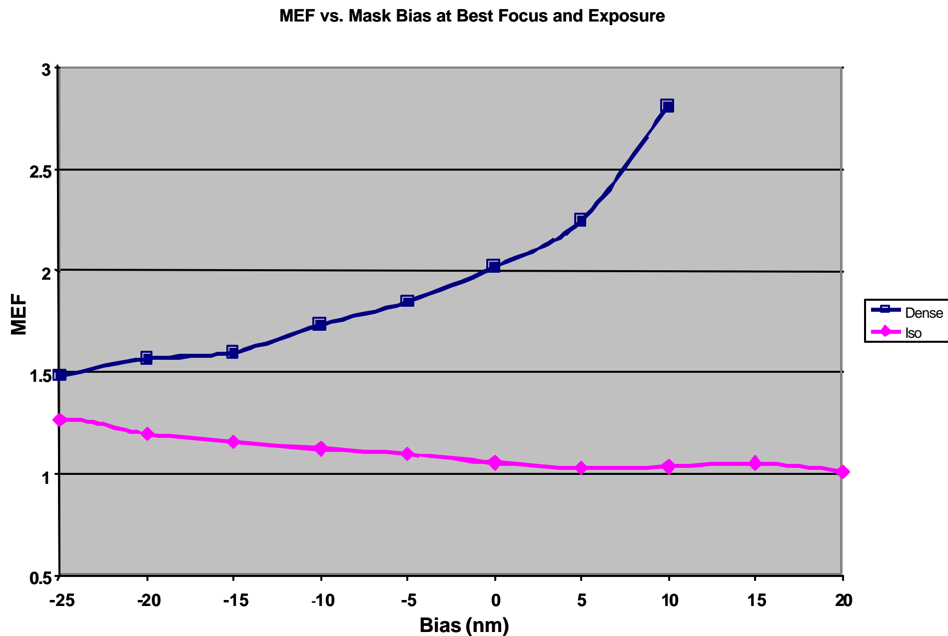

Figure 3: MEF vs. mask bias at best focus and exposure for isolated and dense lines.

Just as the MEF is a strong function of feature size and pitch, it also depends strongly on processing conditions. Fig. 4 shows the MEF for dense lines and spaces as a function of focus and exposure. While the MEF is a tolerable 1.7 at best focus and exposure, it balloons rapidly to values > 3 for a slight positive defocus and/or underexposure, both of which make it more difficult to clear the small spaces between the lines. Note that the MEF actually improves with overexposure, although in this case the resist lines would become smaller than intended for all linewidths on the reticle. For semi-dense features (linewidth 180/space 240 nm), the situation is much better (Fig. 5). Near zero bias, the MEF is fairly close to 1.0, although it degrades

slightly with underexposure and/or defocus, and becomes markedly worse as the mask bias becomes larger. Note the increase in MEF as the mask bias moves from near zero to +/- 10 nm; even for the more relaxed case of semi-dense lines, the MEF begins to creep up as the bias grows and process conditions drift.

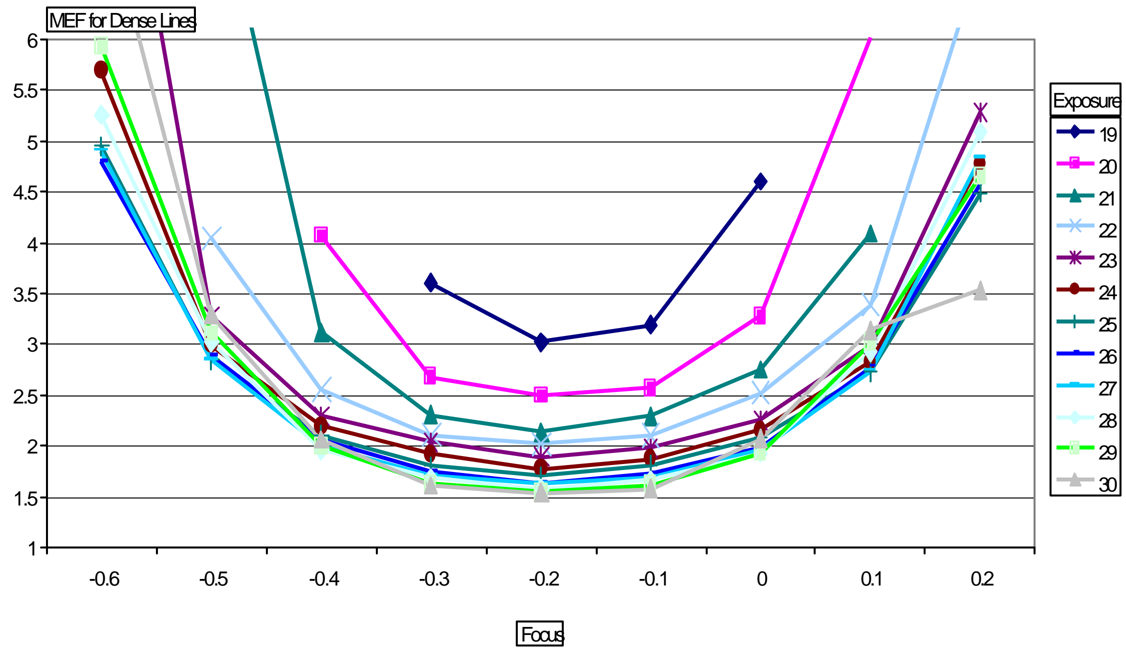

Figure 4: MEF at zero bias vs. focus and exposure for dense lines and spaces; best focus is –0.2, dose to size is 22.5 mJ/cm2.

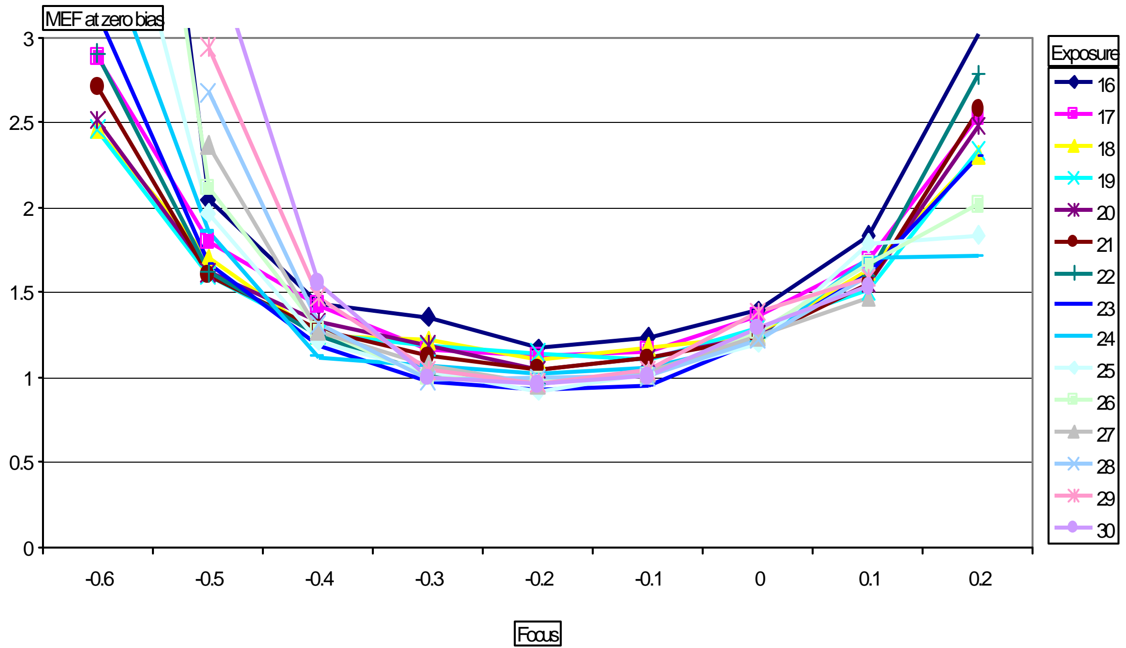

Figure 5: MEF at zero bias vs. focus and exposure for semi-dense lines and spaces; best focus is –0.2, dose to size is 21 mJ/cm2. Note that the y-axis values are half as large as for dense lines.

The increased sensitivity to mask errors as a function of focus, exposure and feature type means that mask specifications can not be determined by simply dividing the desired reticle CD contribution by a fixed MEF value. In order to properly understand the impact of mask errors on a realistic process, the process window proves to be an exceptionally useful tool. Figure 6 shows a simulated process window for 180 nm dense line/space pairs assuming a perfect mask with no CD errors. Sufficient process window exists to print these features with acceptable exposure latitude and depth of focus. What is the impact of a mask error on the process window? Figure 7 shows three process windows: the nominal process plus the imaging results for +5 nm and –5 nm reticle CD errors (wafer dimensions; +/- 20 nm at the reticle). The overlap of these three process windows is significantly smaller than the baseline process.

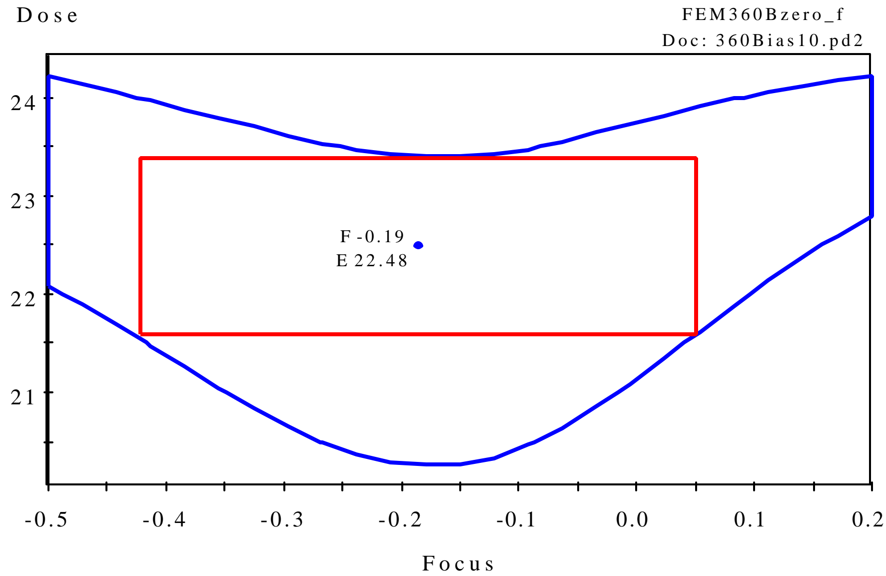

Figure 6: Process window for 180 nm dense line and spaces (360 nm pitch) assuming no mask errors.

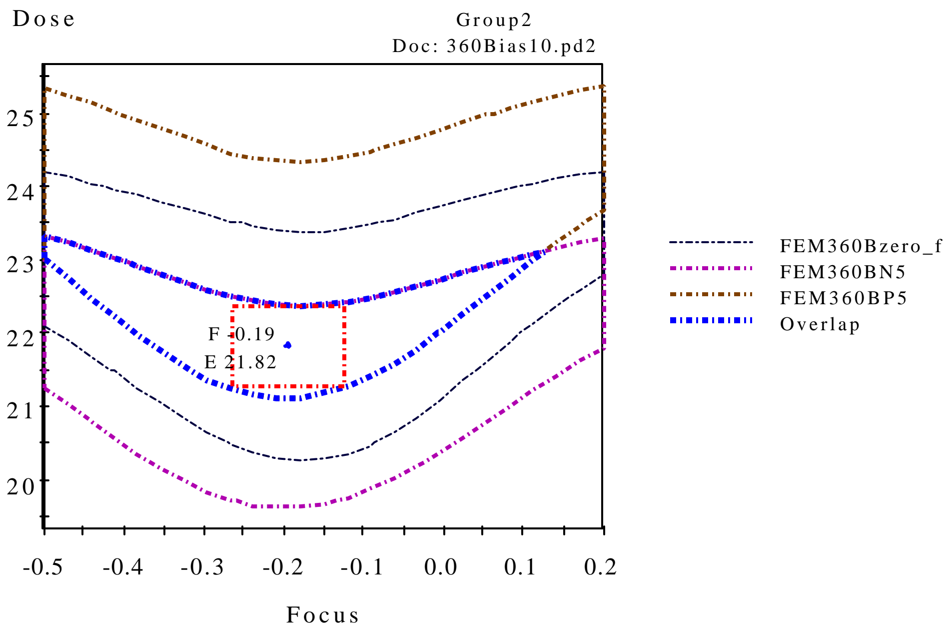

Figure 7: Overlapping process windows for 180 nm dense line/space pairs for perfect reticle (dashed lines) and with +/- 5 nm bias (wafer level: +/- 20 nm at the reticle). Note the sharply reduced process window (central square) compared to figure 6.

Figure 8 shows the analysis of these process windows to produce the exposure latitude versus depth of focus (DOF) curves (a measure of the size of the process window). It is quite obvious that these relatively small reticle CD errors are reducing the size of the process window by more than half! The DOF drops from a respectable 0.7 µm to a painfully small 0.4 µm, and the depth of focus for 8% exposure latitude drops from 0.5 µm to zero. Complete process window qualification for each feature type of interest is required to establish viable reticle CD specifications.

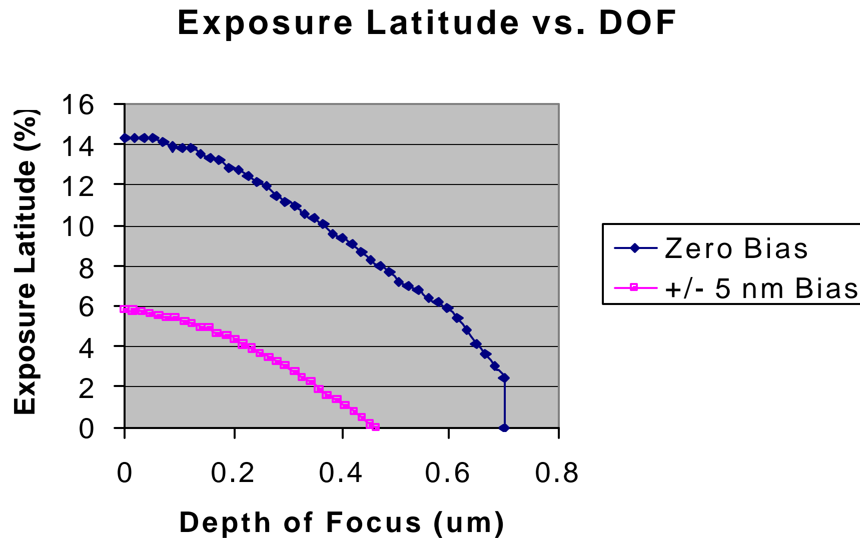

Figure 8: Exposure latitude vs. depth of focus for 180 nm dense line/space pairs. Upper curve: reticle, with no CD errors. Lower curve: reticle with +/- 5 nm CD errors (at wafer level: +/- 20 nm at reticle).

3. SEPARATING RETICLE AND WAFER CD ERRORS

Wafer CD data can be analyzed automatically using Klarity ProDATA software to calculate the common process window across multiple critical features. In addition, the SEM images of the reticle and as-printed features can be overlaid to provide a visual assessment of systematic reticle to wafer pattern transfer effects. Differences in the source and resultant image can be quantified using the Critical Shape Measurement capability available with ProDATA. Finally, MEF values which have been determined from prior experiments or modeling can be applied to the reticle CD data to predict the expected wafer CD pattern. Differences between the expected and measured wafer results indicate other sources of variance which need to be quantified and, if possible, corrected.

Even with the highest speed SEMs available, it would be prohibitively slow to measure wafer data over all combinations of focus, exposure and other critical process parameters. This is where simulation proves its value in bridging the gap between reticle space and wafer space. In this case, the inputs are run through the PROLITH modeling program to predict the expected wafer level results[7]. Calibrating the simulation against experimental data provides confidence that the simulated results will be valid over a much broader and more detailed range of process conditions than are accessible experimentally. The combination of reticle and wafer SEMs and modeling provides the tools needed by both mask shop and wafer fab engineers to fully characterize the impact of reticle CD errors on wafer level process windows, and to use this information to set reticle level CD specifications for even the most advanced processes.

4. RETICLE CD QUALIFICATION

Once the reticle CD specifications have been established, a strategy is needed to verify reticle CD performance. Historically, reticle CD qualification has been done with optical measurements on a limited number of special test structures. While this has been adequate in the past, it is risky – to say the least - to assume that millions of complex device geometries are in spec based on data from a few dozen test sites. The impact of reticle CD errors on the process window shown earlier drives the requirement for systems to detect relatively small CD errors anywhere on the reticle. State of the art reticle inspection systems and algorithms have been developed to detect localized CD errors anywhere within the reticle, however these are error detectors, not metrology tools. The reticle SEMs can measure large numbers of reticle CDs in a reasonable period of

time, but even the SEM can only sample a fraction of the full reticle pattern. A complete solution to reticle CD qualification requires both reticle inspection with advanced CD error detection algorithms and CD-SEM measurement[8]. The inspector covers 100% of the reticle at lower CD resolution; the SEM can sample the reticle with much higher accuracy. Even this combination can not insure that every single feature is within spec, but fortunately the mask making process is fairly uniform. Any error in the writing or etching of the reticle is most likely to cover a large enough area to be captured by the inspection and metrology tools. Careful study of the spatial frequencies of CD variation across the reticle can allow the user to select the SEM sampling frequency for the optimal characterization of the complete reticle CD distribution.

As our brief survey of the MEF showed, different feature types respond quite differently to small errors in reticle CD. We can account for this feature dependence in qualifying reticles by creating test structures with a variable range of pitches located within a single SEM field of view (Fig. 9). The SEM can quickly determine if the reticle CDs are within specification across the entire pitch range. In cases where the reticle CD performance is questionable, a focus exposure matrix can be exposed or simulated with a calibrated model and displayed in the form of overlapping process windows to determine if the reticle will give acceptable results.

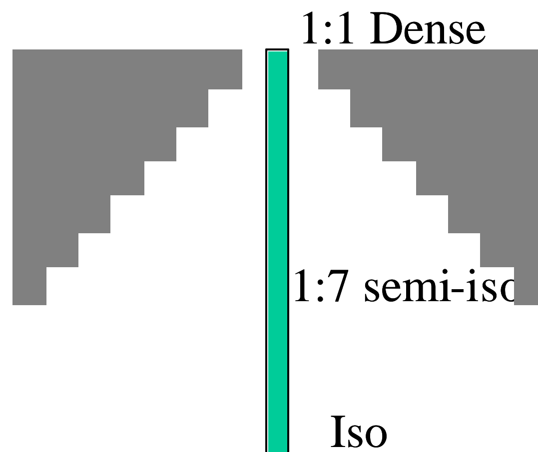

Figure 9: Example of a single test structure with a fixed linewidth and multiple pitches in a single SEM field of view.

5. WAFER LEVEL PROCESS MONITORING

The variable pitch test structure of Figure 9 can be used not only for reticle qualification, but for wafer level process monitoring as well. By tracking the common process windows of the different structures over time, process stability can be insured. The concept of a common reticle and wafer level process window monitor can even be extended by making the tightest pitch in the test structure even denser than the tightest pitch required by the design rules. The test structure can thus provide an early warning of process drifts before they affect the performance of the actual device being manufactured. Even for DRAMs, where 1:1 pitches are common, a superdense test structure can be included in the test pattern where the lines are slightly larger than the spaces for a line/space ratio less than one. Fig. 10 shows the process window results for a 180 nm line/160 nm space pattern compared to a 1:1 180 nm line/space pattern. The superdense pattern was biased by –8 nm at the reticle to make the dose to size the same for both patterns, resulting in a 172 nm line/168 nm space pattern at the reticle. The CD of the denser test pattern changes more rapidly as a function of focus and dose, resulting in a tighter process window and providing a more sensitive test of process stability than the actual device itself.

Historically, CDs at the wafer level were measured on simple tuning fork type structures. As process control became more critical, users began to demand test structures that looked more like the actual device geometries, either by creating more circuit-like scribe line test patterns or by moving the CD measurement into the die. With the ever shrinking size of the available process window, even these monitors can be insufficient to detect small process drifts. In fact, process engineers spend a great deal of effort making the critical features in the devices deliberately insensitive to minor process variations. While this is good for yield, it makes the realistic test structure a good indicator of product performance – a product or device monitor – but a poor indicator of process drift. Structures like the superdense pitch target may serve as better process monitors for detecting small drifts in the process before they impact product yield. Carefully selected process monitors can

even be designed to separate out the contributions from different process drifts, such as focus or exposure, and thus provide not just an early warning system but also a specific corrective action to return the process to the baseline condition[9].

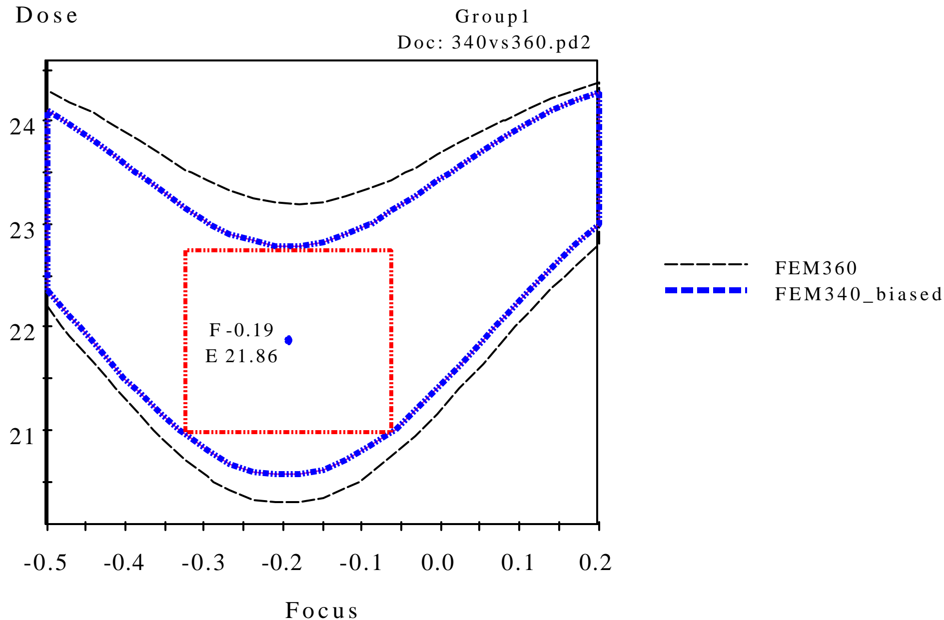

Figure 10: Overlapping process windows for dense line/space pairs on a 360 nm pitch (dashed line) vs. 340 nm pitch (solid line). The tighter pitch has a reduced process window centered within the larger process window, creating a sensitive process monitor.

6. THE ROLE OF OPTICAL EXTENSIONS

Optical extensions, particularly optical proximity correction (OPC), are now being used extensively in production processes at 180 nm and below. In essence, OPC is the inverse of MEF. While MEF is a passive metric of how unintentional mask errors affect the wafer CDs, OPC deliberately alters the reticle CD as a function of feature type, size, and pitch to achieve overlapping process windows for all of the features being printed. The variations we have seen in the MEF as a function of process conditions also affects OPC processes. As a result, OPC models can not be developed without taking into account the expected level of reticle CD variation. The best OPC corrections may not necessarily be those which provide the greatest process window overlap assuming perfect reticles, but rather those corrections which provide the largest common process windows across the full range of expected reticle CDs.

The combination of reticle and CD-SEMs and simulation is also a powerful tool for calibrating optical extension processes and developing the rules and models used to apply these extensions to product reticles. A large part of the difficulty in implementing optical extensions is their sensitivity to numerous process variables, and the dynamic variations in these parameters even in the best fabs. As a result, the process conditions which prevail when production designs are manufactured may be subtly different from those that existed when the calibration was performed. The calibration cycle must be performed over a wide enough range of process conditions to insure that the extensions applied to product reticles will result in acceptable wafer patterns over a maintainable process window, not just under ideal exposure conditions. Analysis of these calibration lots allows the user to predict which specific types of OE structures have the narrowest process windows. Manufacturing insertion of optical extensions requires the implementation of effective monitoring procedures to insure that even these most critical features will be printed correctly.

Another difficulty in implementation is that even if the optical extensions are perfectly optimized for adequate process windows, this does not guarantee that the actual reticle will be a perfect reproduction of that design[10]. Many OPC features are extremely small assist features, such as scattering bars, serifs and other sub-resolution structures, or very small programmed

changes in linewidth for specific features. The fidelity of the mask writing process for these features is not perfect[11]. Structures that were supposed to be sharp will become rounded, and both the width and area of the assist features may be far from the design values. Phase shift masks also require additional characterization, especially for multi-phase reticles. Small phase errors can result in unacceptable CD errors; larger phase errors will print as defects. Qualifying production reticles requires a combination of state of the art reticle inspection tools and reticle CD-SEMs to measure and verify the fidelity of even sub-resolution optical extensions.

7. THE SYSTEMS APPROACH TO RETICLE QUALIFICATION

Hardware and software are critical to developing reticle solutions, but tools alone are not enough. Meeting the evolving demands of reticle qualification requires a greater level of cooperation and mutual involvement by both mask shop and wafer fab engineers. Mask shops are judged by the number of revenue producing reticles they ship, while fabs are judged on the number of good die they produce. Both constantly strive to maintain their costs at the lowest practical level. These pressures can often create conflicts between the need to control reticle costs and the need to achieve the highest reticle quality to improve wafer yield. The increasing technical demands of today's leading edge reticle processes do not allow us the luxury of treating the mask shop and wafer fab as separate entities with different, sometimes competing, economic motivations. Mask and fab engineers will need to work closely to develop production worthy optical extension processes, CD error budgets, and reticle qualification procedures. The interactions between fab process parameters and reticle CD variations will even drive mask shops to tailor the mask making process for specific end users and applications. As Bill Arnold, Executive Scientist of ASML, stated recently[12], ``The day of the reticle as a commodity has passed, and all elements of the lithography system need to be engineered to the highest performance levels for successful wafer image formation". Hardware and software provide the tools, but engineers in both the mask shop and the wafer fab will need to be to use these tools together to successfully address the challenge of engineering the complete lithography system.

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