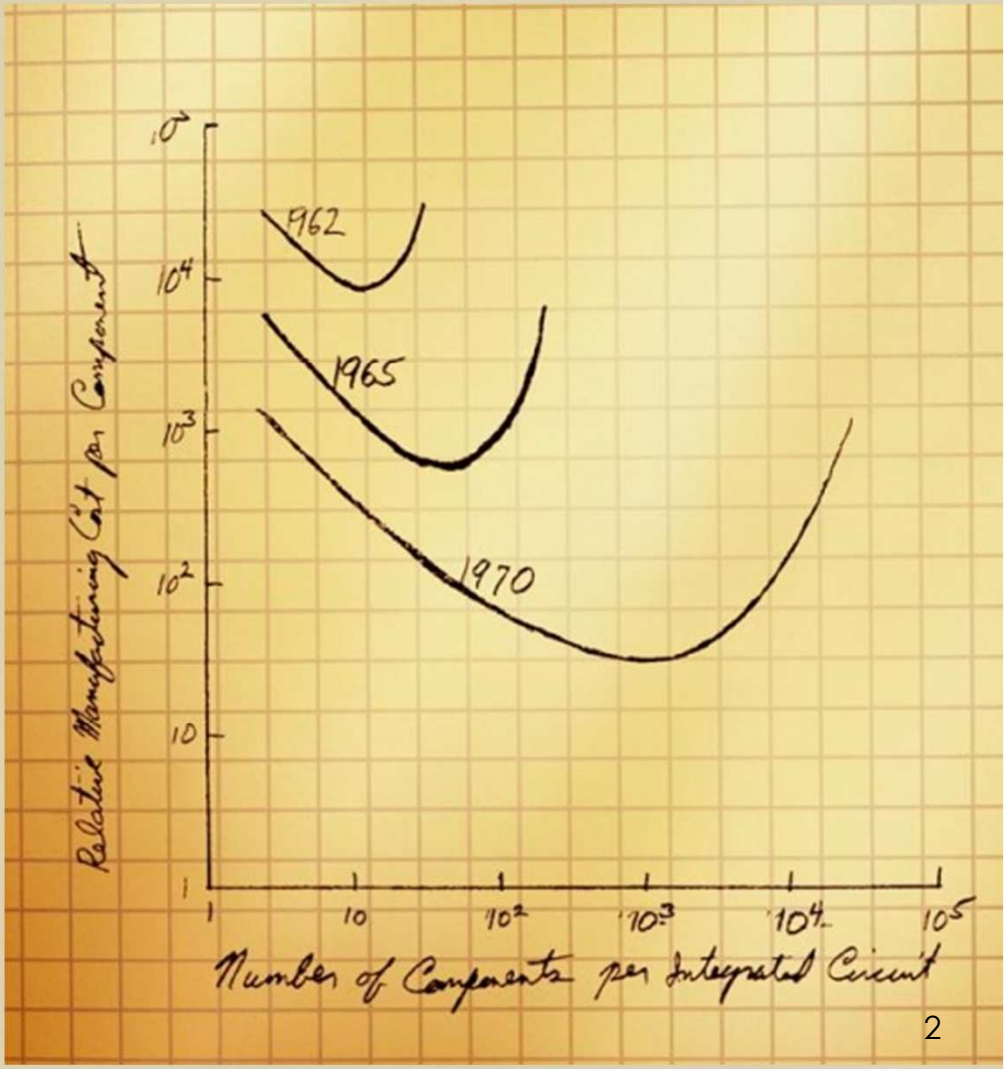
The future of lithography and its impact on design

Chris Mack

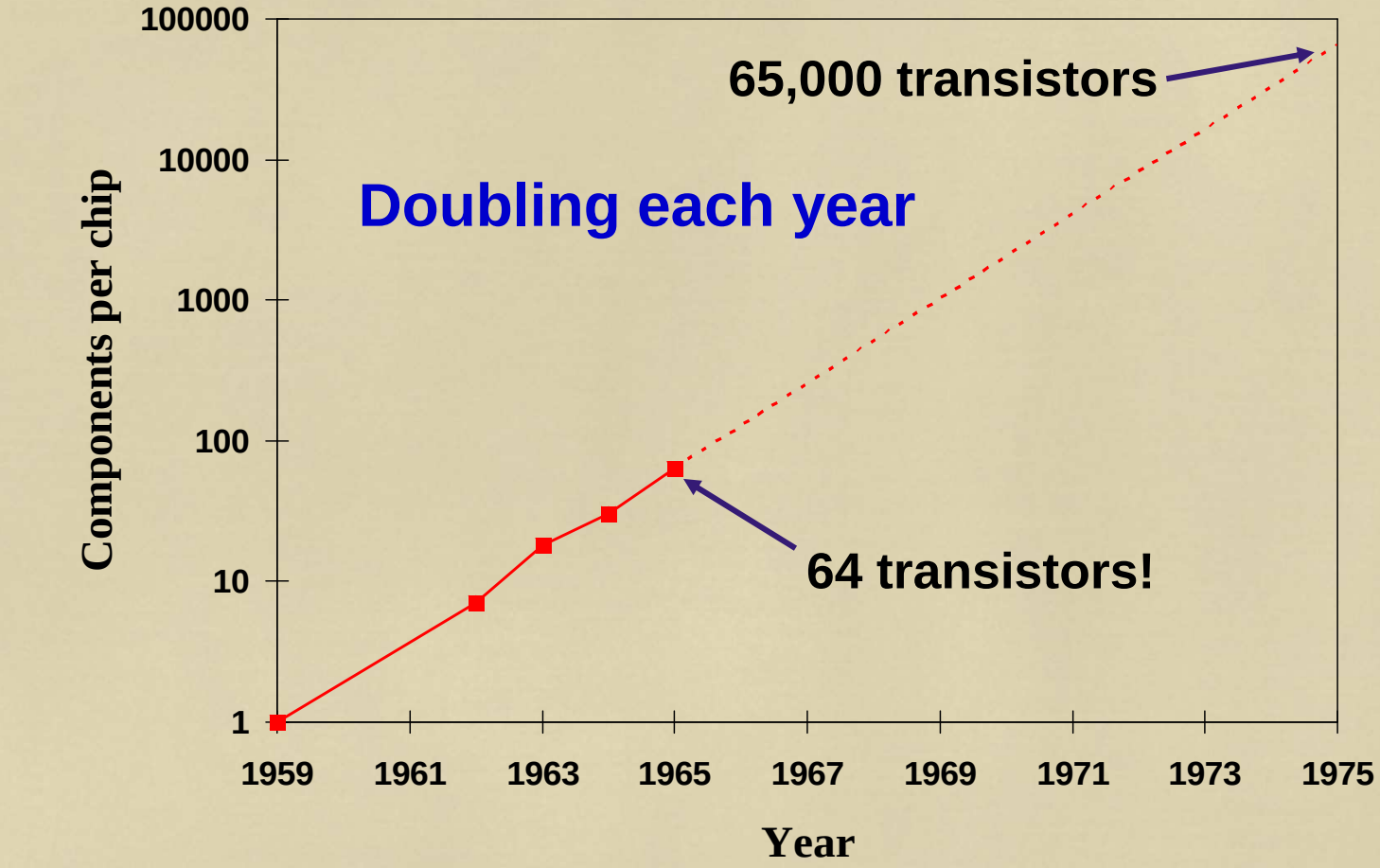
www.lithoguru.com

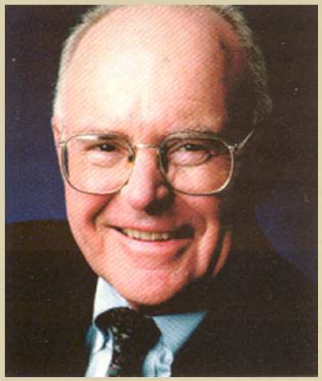
Outline

- History Lessons
  - Moore's Law
  - Dennard Scaling
  - Cost Trends
- Is Moore's Law Over?
  - Litho scaling?
- The Design Gap
- The Future is Here



1965: Moore's Observation

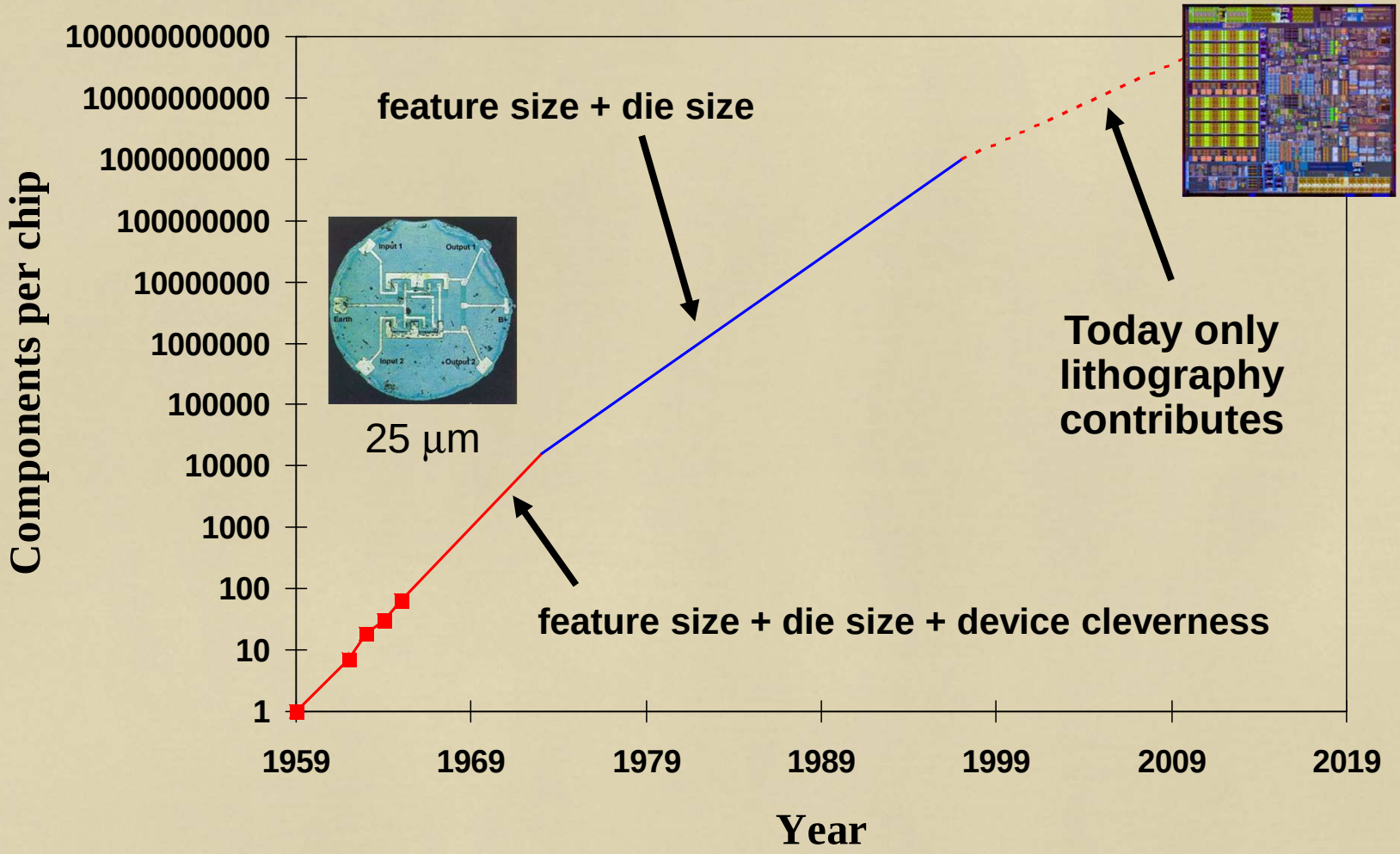




G. E. Moore, "Cramming More Components onto Integrated Circuits," *Electronics* Vol. 38, No. 8 (Apr. 19, 1965) pp. 114-117.

Moore's Law

"Doubling every 1 – 2 years"



Dennard's MOSFET Scaling Rules

Robert Dennard

Device/Circuit Parameter	Scaling Factor
Device dimension/thickness	$1/\lambda$
Doping Concentration	λ
Voltage	$1/\lambda$
Current	$1/\lambda$
Capacitance	$1/\lambda$
Delay time	$1/\lambda$
Transistor power	$1/\lambda^2$
Power density	1

There are no trade-offs. Everything gets better when you shrink a transistor!

IEEE Journal of Solid-State Circuits, Vol. SC-9, October 1974, pp. 256-268.

The Golden Age
1975 - 2000

- Dennard Scaling - as transistor shrinks it gets:
  - Faster
  - Lower power (constant power density)
  - Smaller/lighter
- Moore's Law
  - More transistors/chip & cost of transistor = –15%/year
    - More powerful chip for same price
    - Same chip for lower price
  - Many new applications – large increase in volume

Problems with Dennard Scaling

- Voltage stopped shrinking 10 years ago
  - Thermal noise (kT/q = 25 mV at room temperature)
  - Subthreshhold leakage current
- Gate oxide can only get so thin
- Interconnect dominates delay
- Power is at a wall
- Transistor variability grows with smaller size
  - Small number of dopants per transistor, LER
- Today, shrinking a transistor makes it worse

Dennard + Moore Today

- The only benefits of shrinking a transistor today are lower cost/function and more functions/chip
- Moore's Law cost: despite rising fab, equipment and material costs, and increasing process complexity, the cost/cm^2 of finished silicon has remained about constant over the years. How?
  - increasing yields
  - increasing equipment productivity
  - increasing wafer sizes

Chip Yield Trend

- 1970s
  - High volume yields of 20 – 40%
- 1980s
  - High volume yields of 40 – 60%
- 1990s
  - High volume yields of 70 – 90%
- 2000s
  - Yields must stay high, even as the technology gets more difficult (very hard to do!!)

Lithography Costs
(single patterning)

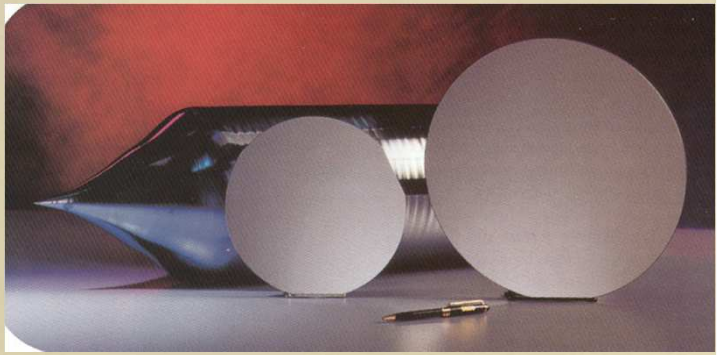
	1979 g-line stepper	2004 ArF scanner	2012 ArF scanner
Wafer diameter (mm)	100	300	300
Tool throughput (wph)	18	100	240
Area throughput (cm^2/sec)	0.39	20	47
Tool cost (M$)	0.45	20	50
Tool cost (¢/cm^2)	0.65	0.65	0.67

(Note: this scaling requires that demand for chips increase by 100X)
(Assumes 5-year straight line depreciation, maintenance not included)

Wafer Size Trend

- Time between wafer size increases is growing:

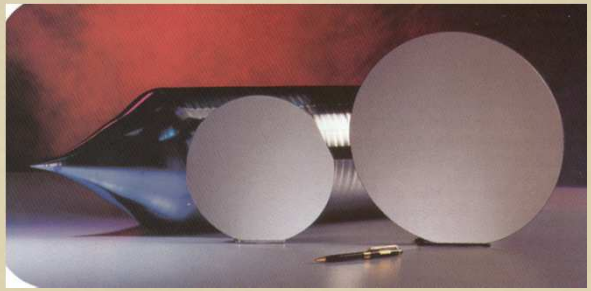
Year*	Wafer Diameter
1969	3 inch
1976	4 inch
1984	5,6 inch
1989	200mm
2000	300mm

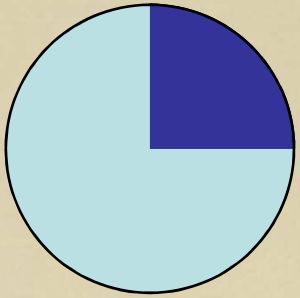


*first year of major production

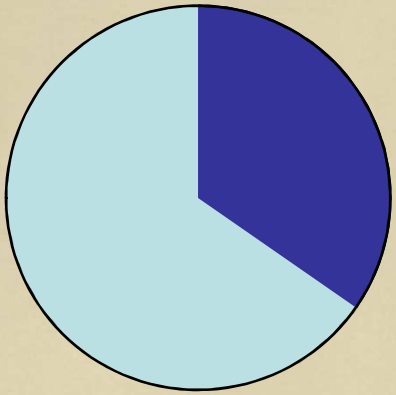
Wafer Size and Litho Costs

- Litho costs scale with area, not wafers
- Increasing wafer size means litho costs increase as a fraction of total costs

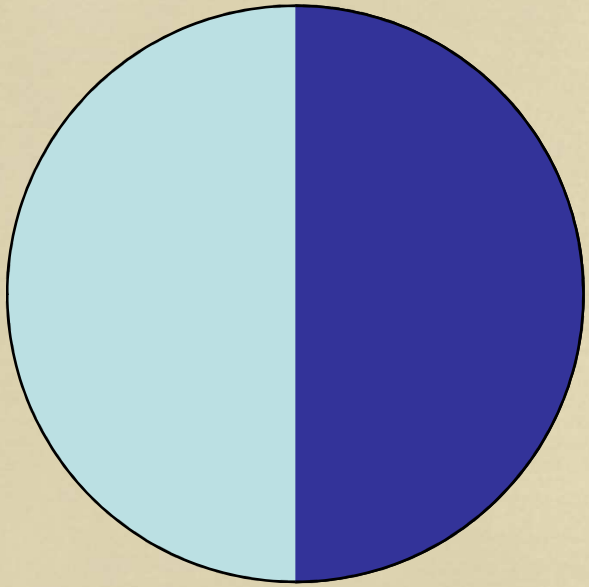




150 mm wafer
25% Litho Cost



200 mm wafer
33% Litho Cost

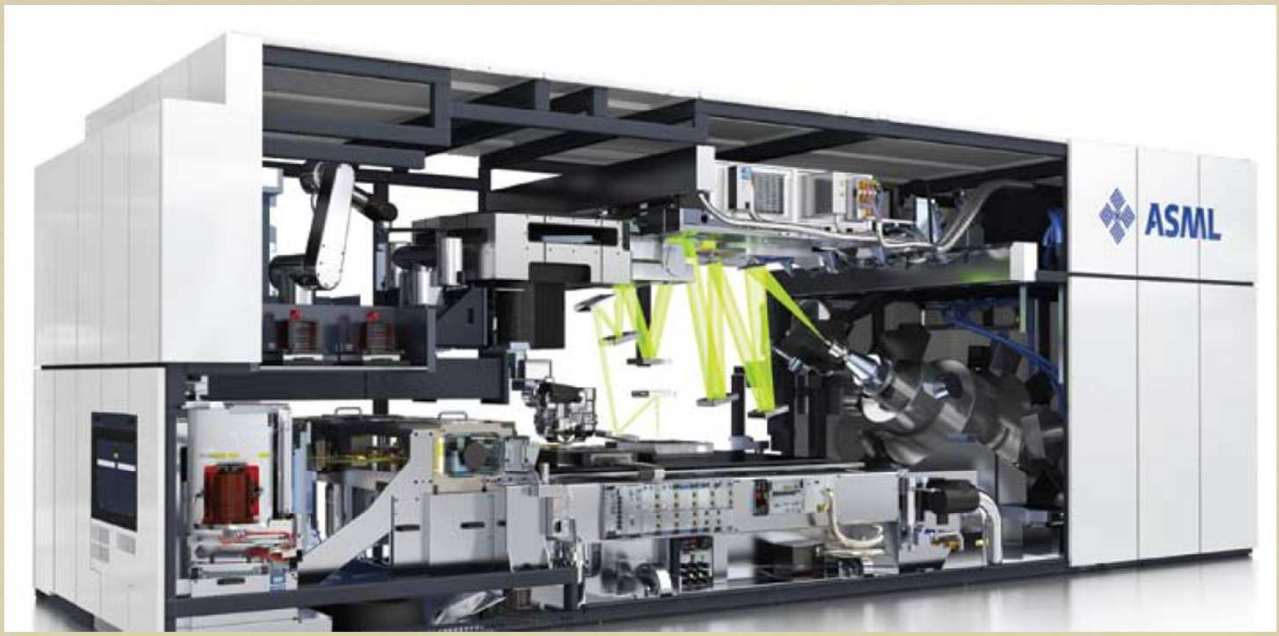


300 mm wafer
50% Litho Cost

Litho Costs are Rising

- Wafer costs are very sensitive to litho costs
- Today, resolution improvements come ONLY from multiple patterning
  - Litho costs must rise with multiple patterning
- Moore's Law costs scaling is no longer -15%/yr
  - What is the smallest cost/transistor improvement that makes the next node worth while?

EUV Lithography



	NXE:3100	NXE:3300B
NA	0.25	0.32
Illumination	Conventional, 0.8σ	Conventional, 0.2-0.9σ
Off-axis as an option		
Resolution	≤ 27 nm	≤ 22 nm
Field size	26 x 33 mm	26 x 33 mm
Single-machine overlay (SMO)	4.5 nm	3.5 nm
Matched machine overlay (MMO)	7.0 nm	5.0 nm
Throughput	60 wph	125 wph
Resist dose	10 mJ/cm²	15 mJ/cm²

← Currently 10 wph

EUV Lithography: the Future is Not Bright

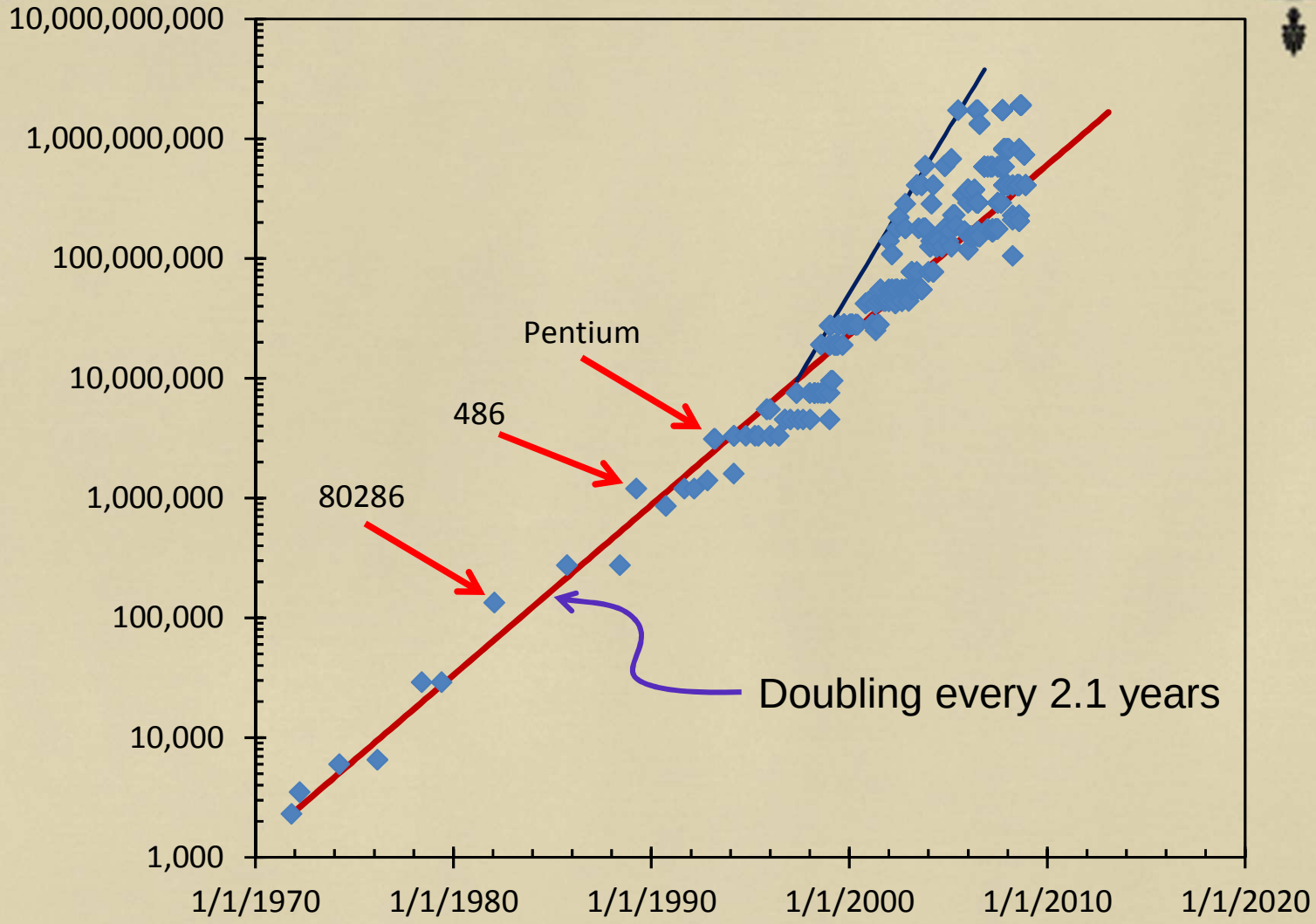
- Three major roadblocks to EUVL production
  - Defect free masks (yield)
  - High brightness source (throughput)
  - Low line-edge roughness (LER)
- Current schedule calls for NXE:3300 shipping this year, going into production next year at 70 wph
  - This will not happen
- In the end, it is the economics of production with EUVL that will determine its fate

The End of Litho Scaling?

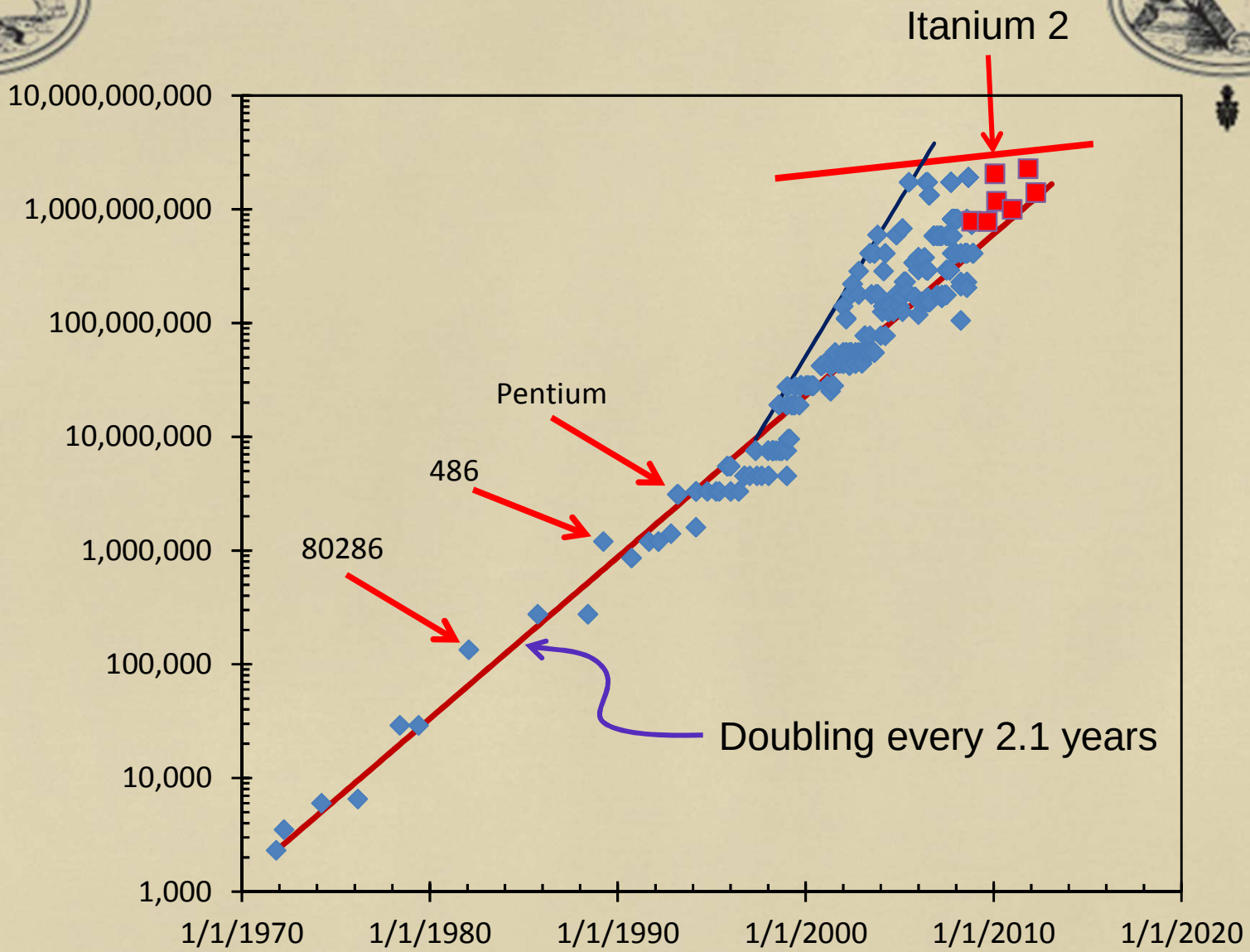
- The reason to scale feature size is to lower the cost per transistor
- But if litho costs continue to rise, this benefit will likely disappear
  - If higher litho costs mean higher cost per transistor, why reduce feature size?

But wait! What about Moore's Law?

Intel's Moore's Law

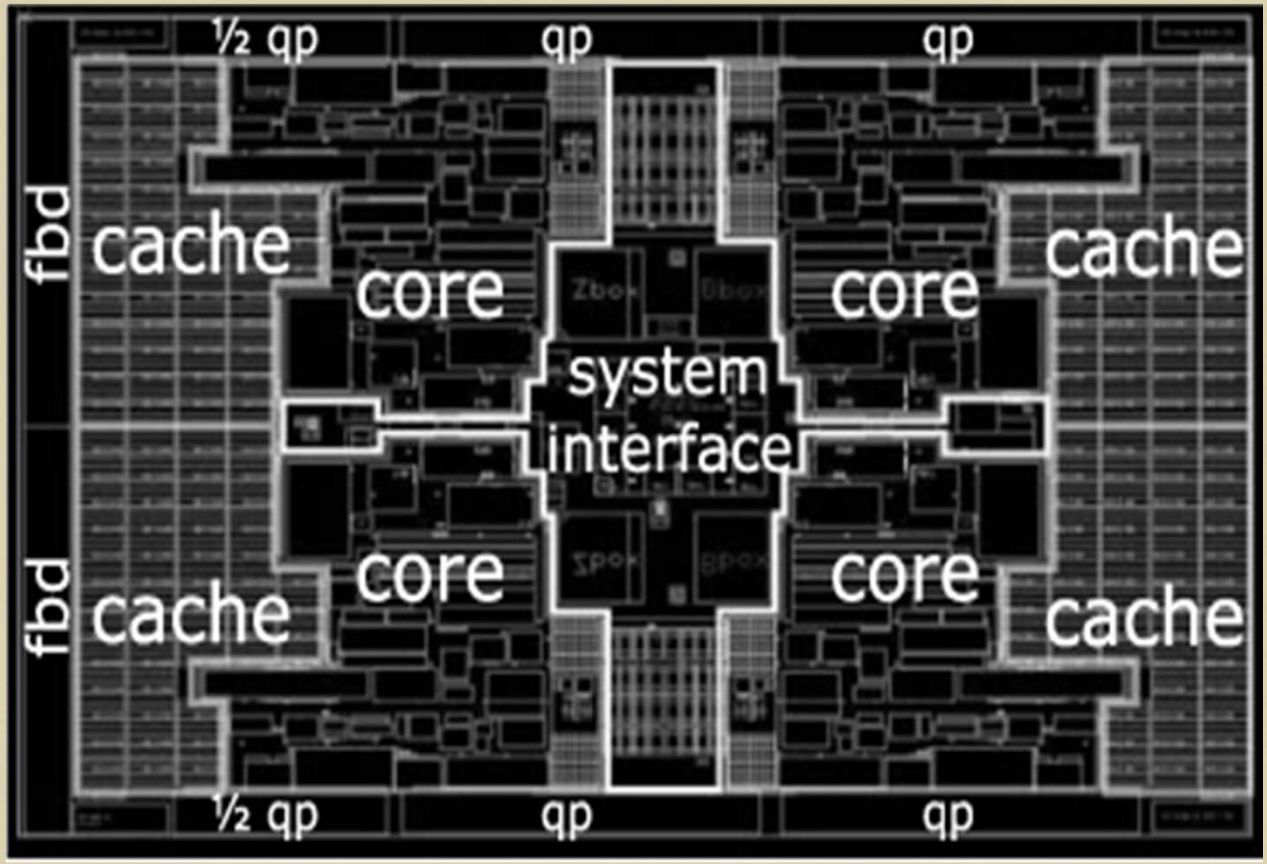


Intel's Moore's Law

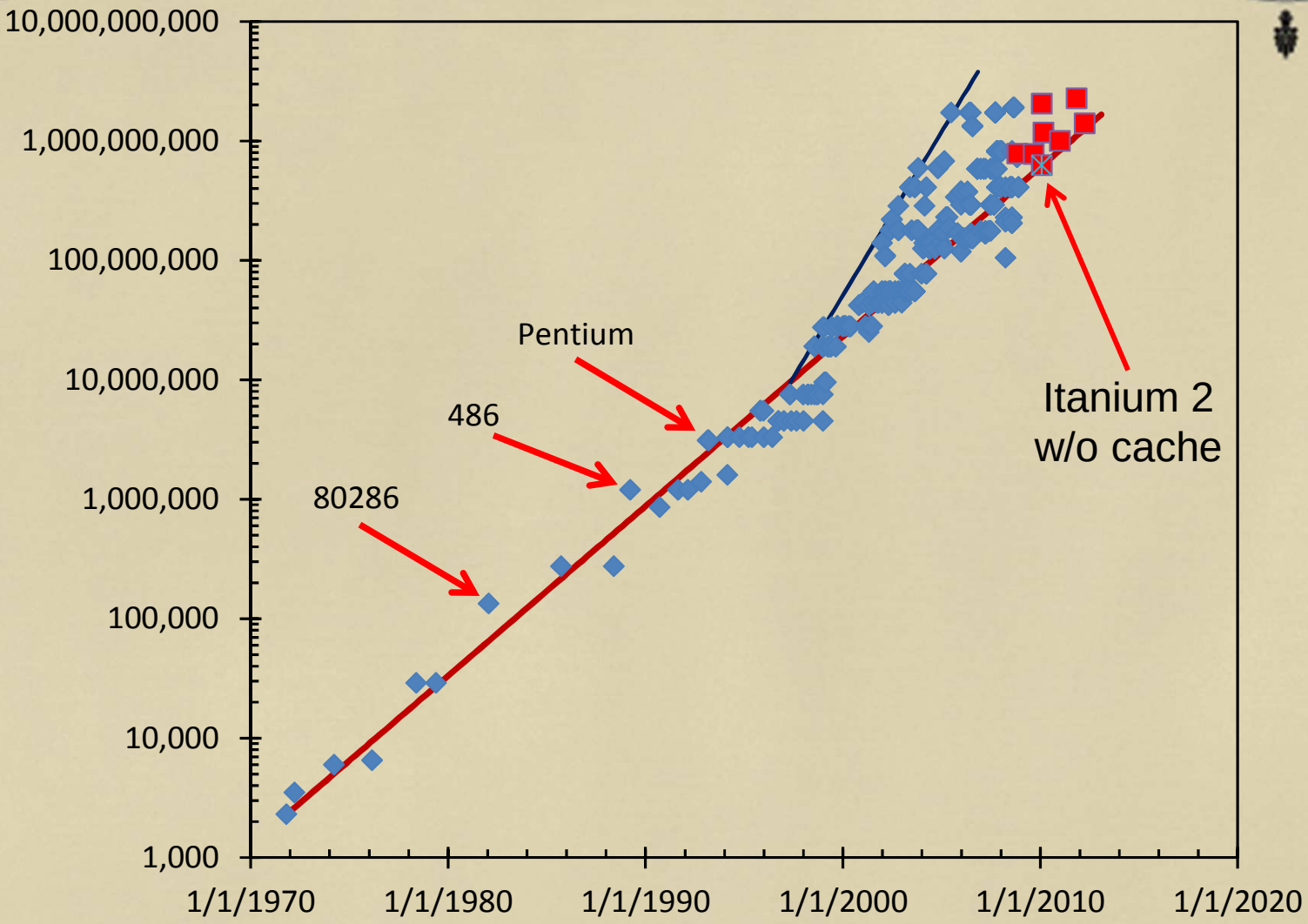


Intel's Itanium 2

- Introduced Feb. 2010
- First Intel chip with 2 billion transistors
- 30MB Cache (1.4 billion transistors)



Intel's Moore's Law



The Design Gap

- Today, we can make more transistors than we can use in logic circuits
  - The trend in microprocessors is multiple processors per chip with lots of cache and SOC
  - Typical chip die size is far smaller than maximum
- For logic, the only reason to shrink today is cost
  - We are simply not using more transistors
- Flash memory has no problem using as many transistors as we can make
  - so long as the cost per transistor keeps dropping

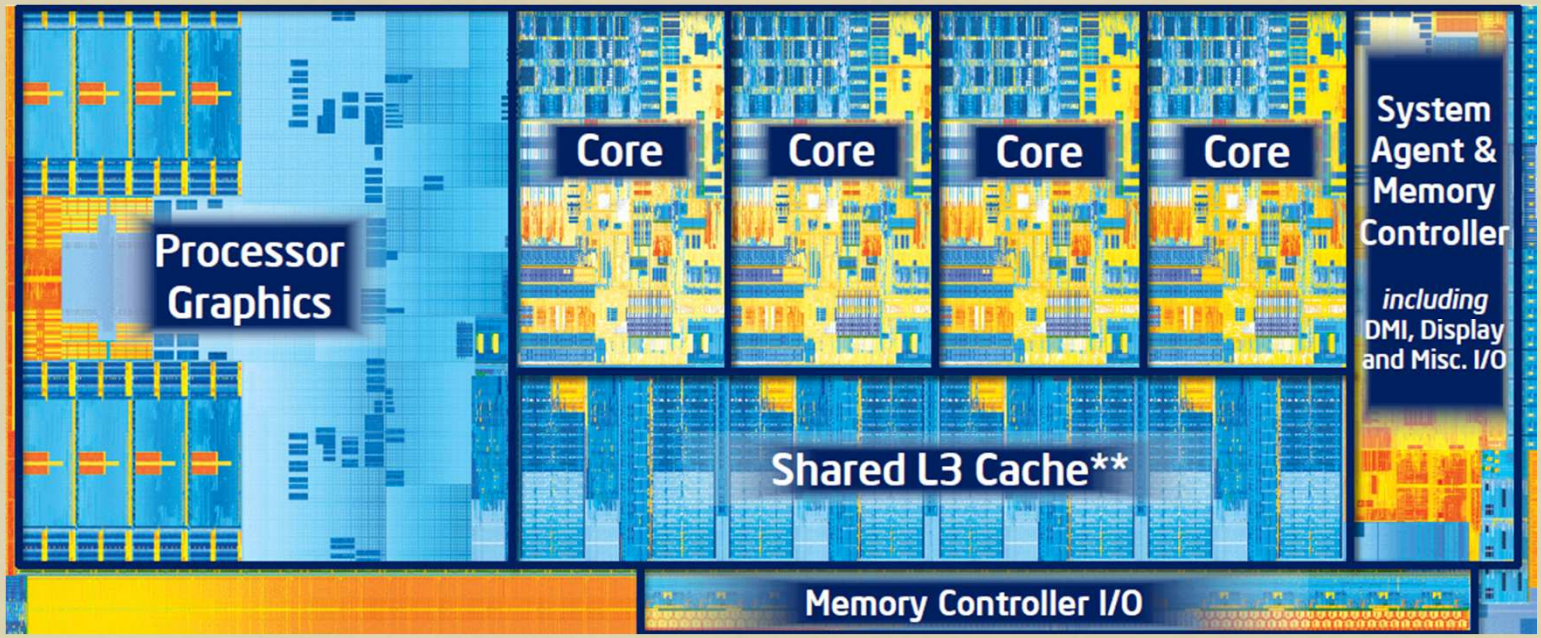
The Design Gap

$$\text{Design Gap} = \frac{\text{\# transistors/chip I can make}}{\text{\# transistors/chip I can design}}$$

Design Gap

Intel Ivy Bridge

- 22-nm process
- 1.4 billion transistors
- Shrink from 32-nm Sandy Bridge

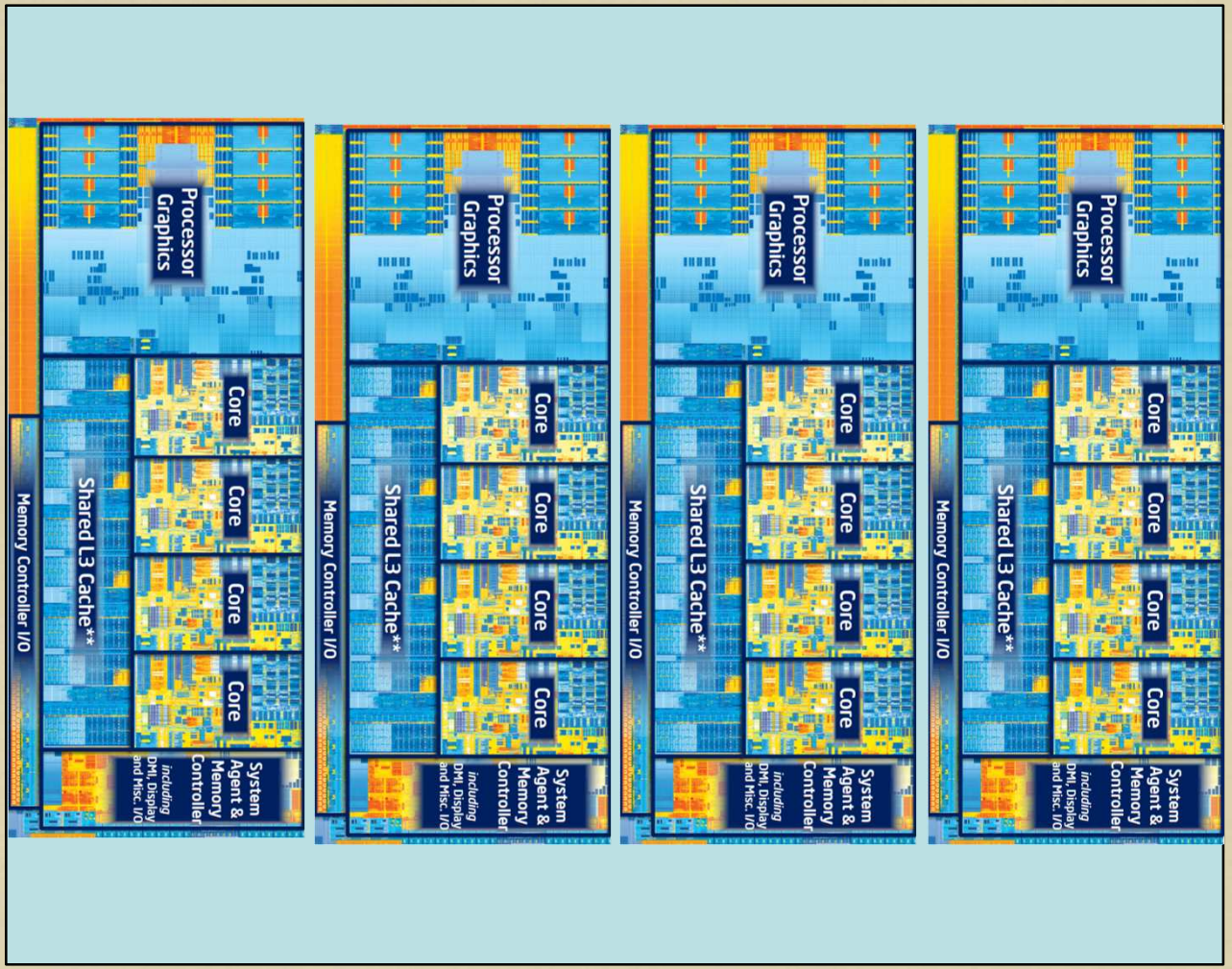


8.14 mm

19.5 mm

Design Gap

Maximum Lithography Field Size

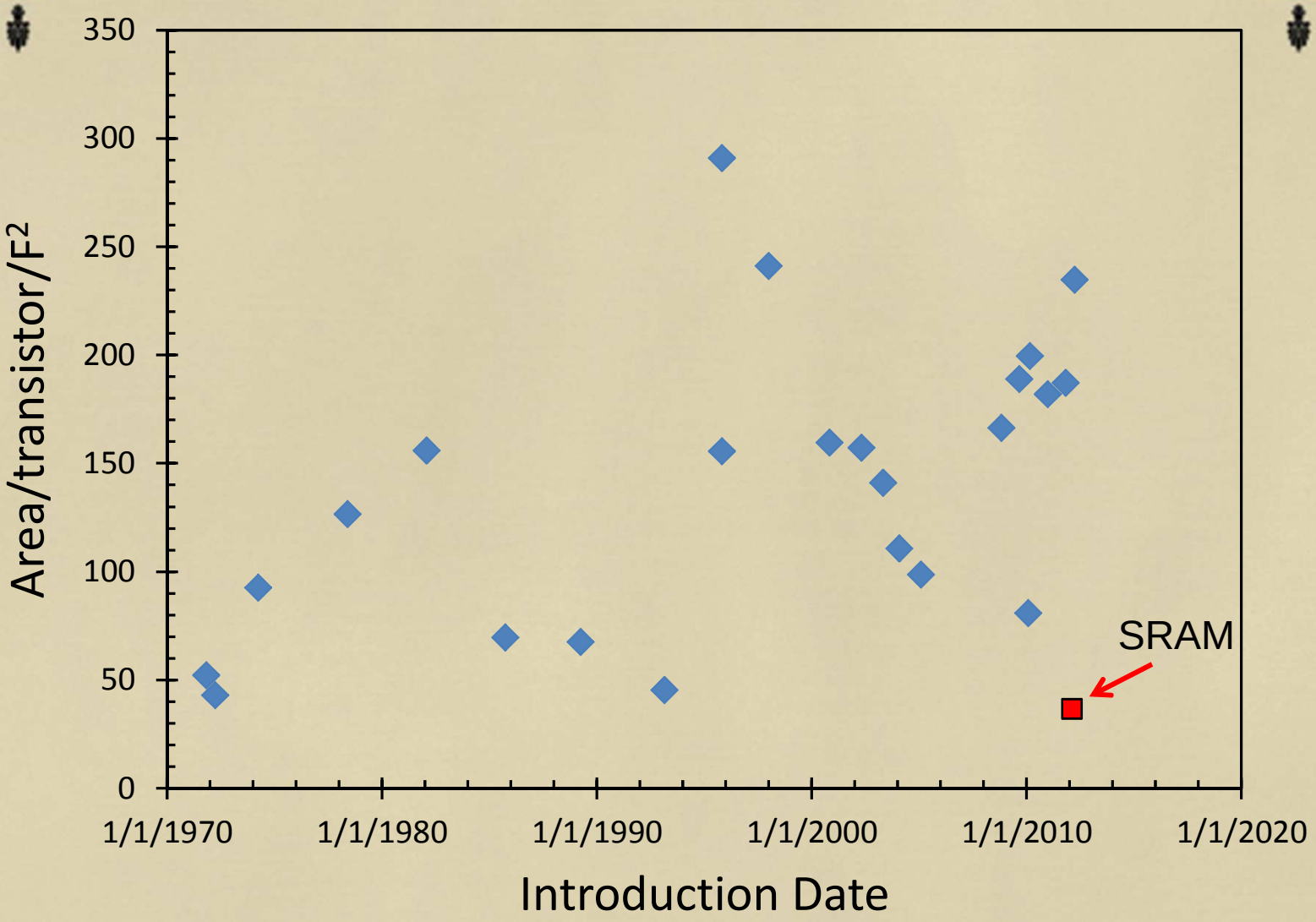


Device Cleverness

How to reduce the area per transistor

- Isolation: LOCOS → STI (shallow trench isolation)
- Interconnect: Single metal (all tracks between transistors) → Multilevel metal (most tracks above transistors). Has this shrunk area/transistor?
- Transistor: Planar → FinFET (gate width into the third dimension)
- DRAM: Folded bit line ($8F^2$) → Diagonal bit line ($6F^2$)
- Flash: Single level cell → Multilevel cell

Intel Microprocessor Device Cleverness



The Future: "Standard" Scenario

- Begin using EUV lithography in 2014
  - Many technical hurdles
  - May never be cost-effective: the SST of lithography?
- Wafer size increases to 450 mm in 2017 - 2018
  - Lowers the cost per chip, but only for high-volume manufacturers
  - No one knows how to pay for the equipment development costs
  - Litho cost becomes 70 – 80% of chip cost
- Chip production is dominated by three or four super-fabs
  - One fab costs > US$10B
- Moore's Law goes on as before
  - We all have a super computer in our pocket

The Future: "Possible" Scenario

- 193i + DSA
  - Very tight (single) pitch unidirectional lines cover the chip
  - Cuts made with 193i + DSA with simple design rules
- Strict layout paradigm
  - All devices are on a grid
  - Layout choice: where to *remove* a line
- There will be no shrink of standard cell IP
  - Every IP block must be redesigned
- Materials challenges
  - High resistance lines and high resistance contacts

The Future: "Likely" Scenario

- Moore's Law continues only by redefining it
  - True Moore's Law ends on Wednesday, Feb. 26, 2014
- Litho is good at printing small lines/spaces, but not irregular patterns
  - The end of shrinks
- Lithography still a key technology, but value moves to materials, devices, and designs
- The design gap is now about 20 – 30 for logic

Conclusions – There is Hope!

- The Golden Days of Moore + Dennard are over
- The beginning of the end of litho scaling is here
  - Chip cost is extremely sensitive to lithography costs, and lithography costs are rising
- Physical limits are stochastic (line-edge roughness), but economic limits will get us first
- But there is hope!
  - There is lots of room for device cleverness
  - Fill in the design gap!