Mask Specifications: It's not getting any easier

Moore's Law, as practiced today by the semiconductor industry, is all about scaling. Feature sizes, overlay errors, operating voltages, drive currents – everything must scale in some fashion to enable the next generation of device technology. In lithography, as for semiconductor device manufacturing in general, the most basic unit of scaling is the minimum half-pitch on the device. Since the most important benefit of scaling is the ability to pack more transistors into a smaller area, the minimum half-pitch serves as the best (simple) measure of packing density, and thus overall scaling productivity.

But not everything scales at the same rate. Some parameters (such as voltage) scale more slowly, while others (such as photomask dimensional uniformity) scale more quickly. In this article, I'll look at a few mask manufacturing specifications, and show how and why those specifications are scaling at a significantly faster rate than the minimum half-pitch of the device.

In late 2007, the 8th edition of the *International Technology Roadmap for Semiconductors* (ITRS) was completed. The first "official" roadmap, the SIA's *Semiconductor Technology Workshop Conclusions*, was published in 1993 based on a workshop held in Irving, Texas in November, 1992 (the document wasn't called a "roadmap" until its second edition, in 1994). The stated goal of the workshop was to "…create a common vision of the course of semiconductor technology over the next 15 years." Since 1997, this roadmap has been updated every two years. While each edition of the roadmap serves to predict the pace of the industry for the coming 15 years, the collection of these eight roadmaps also serves to show the actual pace that the industry has taken, since each roadmap begins with a snapshot of the industry status.

For example, Table I shows mask data extracted from the last seven roadmaps. For any given roadmap edition, the roadmap data from the report always begin with the roadmap year, and then make projections into the future. In Table I below, I ignore the projections made in the roadmap reports, and simply extracted the current year's data (for example, the 2001 data comes from the 2001 edition of the roadmap). Thus, we have a very simple method for capturing lithographic trends over the last ten years.

Table II and Figure 1 show the relative scaling rates of several mask specifications over the last 10 years. Minimum half-pitch has shrunk by a factor of 4 over that time period, while gate CDs have shrunk somewhat faster (almost a factor of 5). Thanks to OPC, however, the minimum (primary) feature size on the mask has shrunk faster still – more than a factor of 6 in the last 10 years. But it is the critical dimension uniformity (CDU) specification for the mask that has scaled the fastest. Contact hole CDU specs have shrunk by a factor of 14 in the last 10 years – that's more than three times faster than the rate at which the minimum half-pitch has scaled. While everything in lithography becomes harder over time, mask makers have earned more than their share of difficulties.

What happened to cause mask specifications to shrink significantly faster than wafer dimensions? There are three main reasons. In 2000, the industry discovered the mask error enhancement factor (MEEF), where a given percent change in mask CD results in a much higher percent change in wafer CD. As a result, mask CDU specifications shrank by a factor of 2 – 3 to compensate for MEEF (contact hole MEEF being the highest). By 2002, aggressive RET/OPC caused mask primary features to shrink faster than wafer dimensions. And by 2004, double exposure processes put more burden on mask image placement.

How will these mask specification trends play out in the near future? MEEF is getting higher (lithographers now discuss values between 4 and 6 with a straight face), so that we can expect mask CDU specs to continue to shrink significantly faster than wafer CD. Additionally, it is likely that some form of double patterning will become mainstream in the next few years. Depending on the flavor adopted, we could see a significant tightening of mask image placement specifications beyond the normal scaling (by up to a factor of 3). Masks have gotten much harder to make in the last 10 years, even relative to the difficulties in wafer lithography. More of the same is in store for at least the next 5 years.

Roadmap Year	**1994/5**	**1997**	**1999**	**2001**	**2003**	**2005**	**2007**
Wafer min. half pitch (nm)	350	250	180	130	100	80	65
Wafer min. isolated line (nm)		200	140	90	65	54	42
Wafer min. contact hole (nm)			200	150	115	85	84
Mask min. primary feature (nm)		800	560	360	182	150	119
Mask min. OPC feature (nm)		400	280	180	130	107	85
Image placement (nm)	70	52	39	27	21	9	7.8
CD uniformity (nm, 3 sigma)							
Isolated lines	35 - 50	26	16	7.4	4.6	3.8	2.6
Dense lines	36 - 50	32	24	10.4	9.8	7.1	4
Contact/vias	37 - 50	36	24	8	5	4.7	2.5
Linearity (nm)		40	28	19.8	15.2	13	10.4
CD mean to target (nm)	20 - 40	20	14	10.2	8	6.4	5.2
Defect size (nm)	210 - 280	200	144	104	80	64	52

Table I. Photomask specifications drawn from the current year's data from each of the roadmap editions. The data from the 1994 roadmap was a projection for 1995.

Roadmap Year	**1997**	**1999**	**2001**	**2003**	**2005**	**2007**
Wafer min. half pitch	1.00	0.72	0.52	0.40	0.32	0.26
Wafer min. isolated line	1.00	0.70	0.45	0.33	0.27	0.21
Mask min. primary feature	1.00	0.70	0.45	0.23	0.19	0.15
Image placement	1.00	0.75	0.52	0.40	0.17	0.15
CDU Isolated lines	1.00	0.62	0.28	0.18	0.15	0.10
CDU Dense lines	1.00	0.75	0.33	0.31	0.22	0.13
CDU Contact/vias	1.00	0.67	0.22	0.14	0.13	0.07

Table II. Selected data from Table I normalized to the year 1997.

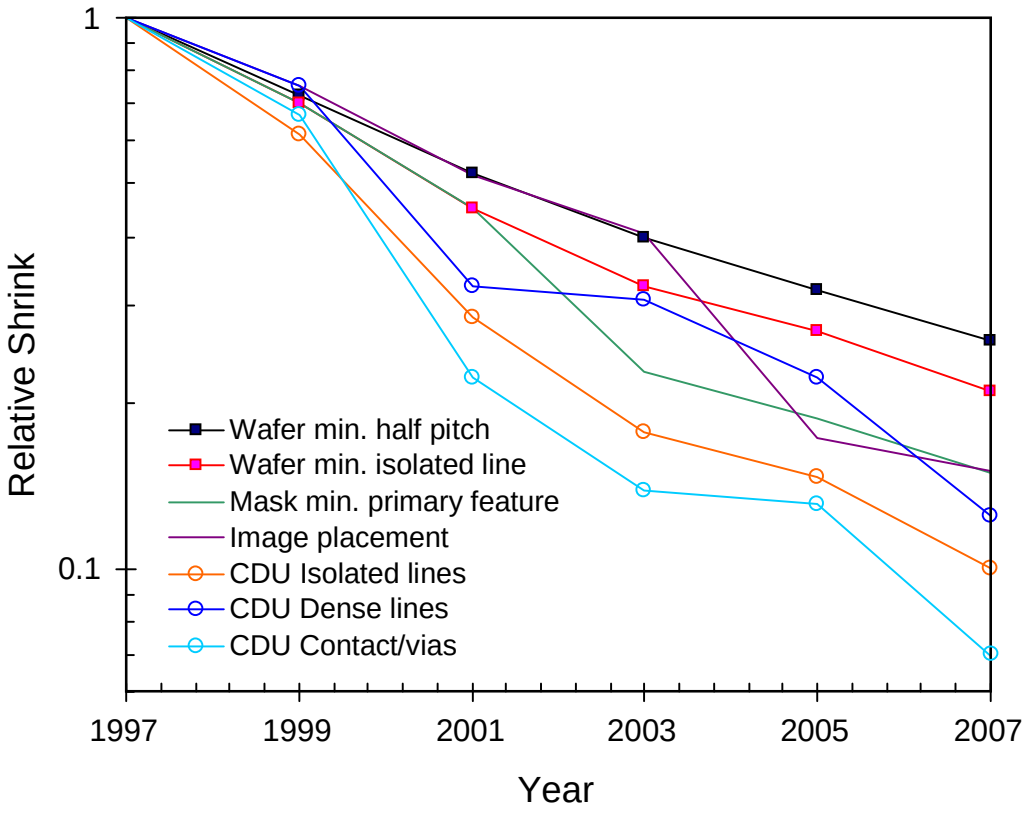

Figure 1. A plot of the data from Table II showing the relative scaling trends for several mask specifications compared to wafer minimum features.