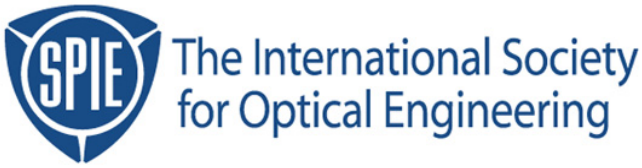

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The End of the Semiconductor Industry as We Know It

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ABSTRACT

The goal of this paper is to discuss the technical and economic drivers of Moore's Law, with special emphasis on their interdependence. These drivers can be classified as "push" (technology improvements push us down the Moore's Law path) and "pull" (economic incentives create increasing chip production volumes which drive the technology learning curve). In fact, Moore's Law can be considered as an instance of general learning curve theory, which places a special importance on the role of increasing chip volumes on the slope of Moore's Law. After a general review of the history of Moore's Law, its relevance today is described in terms of transistor shrinks rather than increasing functions per chip. The challenges required for the continuation of Moore's Law are presented.

Keywords: Moore's Law, learning curve

I. Introduction

The impact of the semiconductor integrated circuit (IC) on modern life is hard to overestimate. From computers to communication, entertainment to education, the growth of electronics technology, fueled by advances in semiconductor chips, has been phenomenal. The impact of these developments has been so profound that it is now often taken for granted: consumers have come to expect increasingly sophisticated electronics products at ever lower prices. The role of optical lithography in these trends has been, and will continue to be, vital.

Underlying the electronics revolution has been a remarkable evolutionary trend called Moore's Law. Begun as a simple observation that the number of components integrated onto a semiconductor circuit doubled each year for the early life of the industry, Moore's Law has come to represent the amazing and seemingly inexhaustible capacity for exponential growth in electronics. In the past forty years this observation we call Moore's Law has grown beyond its original intentions, with the very real danger of loosing its meaning, and possibly is usefulness. What is Moore's Law and how is it useful? What is its relevance to semiconductor trends today? How can its predictability be explained? When will Moore's Law end?

In an attempt to answer at least some of these questions, this paper will begin with a review of the history of Moore's Law, then describe the form of Moore's Law that is most relevant today. Moore's Law will then be explained as an example of an industry learning curve, and a reformulation as "Moore's learning law" will be given. Finally, the coupling of technology innovations to the economic drivers of semiconductor industry growth will allow us to understand the important role of past and future lithography innovations in the continuation of Moore's Law.

II. History of Moore's Law

The remarkable evolution of semiconductor technology from crude single transistors to million-transistor (and now billion-transistor) microprocessors and memory chips is a fascinating story. One of the first "reviews" of progress in the semiconductor industry was written by Gordon Moore, industry icon and a founder of Fairchild Semiconductor and Intel, for the 35th anniversary issue of Electronics magazine in 1965 [1]. After only six years since the introduction of the first commercial planar transistor in 1959, Moore observed an astounding trend – the number of components per chip was doubling every year, reaching about 60 components in 1965 (Figure 1). Extrapolating this trend for a decade, Moore predicted that chips with 65,000 components would be available by 1975! This observation of exponential growth in circuit density has proven to be one the greatest examples of prescience in modern times.

Some important details of Moore's remarkable 1965 paper have become lost in the lore of Moore's Law. First, Moore described the number of components per integrated circuit, which included resistors and capacitors, not just transistors. Later, as the digital age reduced the predominance of analog circuitry, transistor count became a more useful measure of IC complexity. As we shall see next, the accuracy of Moore's extrapolation depends on this definition and a switch to transistor count must necessarily involve a discontinuity in Moore's original trend line. Further, Moore clearly defined the meaning of the "number of components per chip" as the number which minimized the cost per component. For any given level of manufacturing technology, one can always add more components – the problem being a reduction in yield and thus an increase in the cost per component. As any modern IC manufacturer knows, cramming more components onto integrated circuits only makes sense if the resulting manufacturing yields allow costs that produce more commercially desirable chips. This "minimum cost per component" concept is in fact the ultimate driving force behind the economics of Moore's Law.

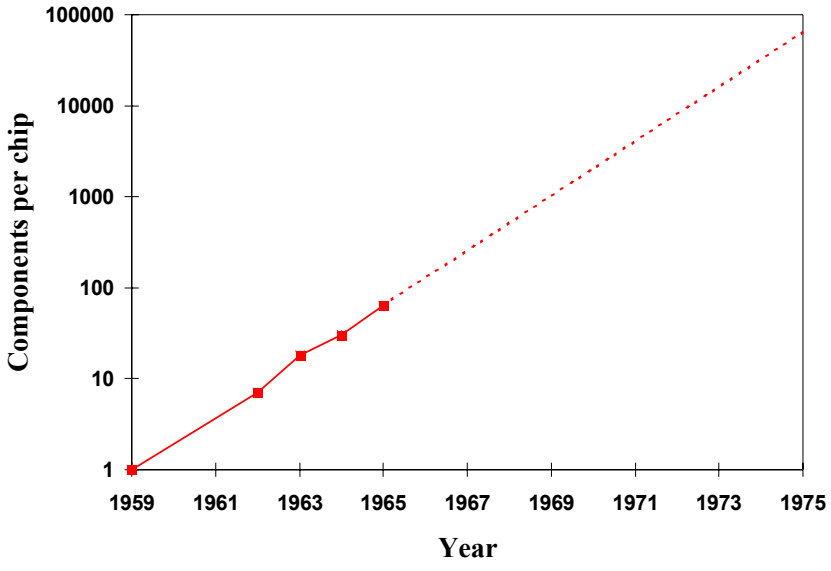


Figure 1. Moore's 1965 prediction of the doubling of the number of components on a chip each year, based on historical data and extrapolated to 1975.

Although extrapolating any trend by three orders of magnitude can be quite risky, Moore's observation proved quite accurate. In 1975 Moore revisited his 1965 prediction and provided some critical insights into the technological drivers of the observed trends [2]. Checking the progress of component growth, the most advanced memory chip at Intel in 1975 had 32,000 components (but only 16,000 transistors). Thus, Moore's extrapolation by three orders of magnitude was off by only a factor of 2. Even more importantly, Moore divided the advances in circuit complexity among its three principle components: increasing chip area, decreasing feature size, and improved device and circuit designs. Minimum feature sizes were decreasing by about 10% per year (resulting in transistors that were about 21% smaller in area, and an increase in transistors per area of 25% each year). Chip area was increasing by about 20% each year. These two factors alone resulted in a 50% increase in the number of transistors per chip each year. Design cleverness made up the rest of the improvement (33%). In other words, the 2X improvement = (1.25)(1.20)(1.33).

Again, there are important details in Moore's second observation that are often lost in the retelling of Moore's Law. How is "minimum feature size" defined? Moore explained that both the linewidths and the spacewidths used to make the circuits are critical to density. Thus, his density-representing feature size was an average of the minimum linewidth and the minimum spacewidth used in making the circuit. Today, we use the equivalent metric, the minimum pitch divided by 2 (called the minimum half-pitch). Unfortunately, many modern forecasters express the feature size trend using features that do not well represent the density of the circuit. Usually, minimum half-pitch serves this purpose best.

By breaking the density improvement into its three technology drivers, Moore was able to extrapolate each trend into the future and predict a change in the slope of his observation. Moore saw the progress in lithography allowing continued feature size shrinks to "one micron or less". Continued reductions in defect density and increases in wafer size would allow the die area trend to continue. But in looking at the "device and circuit cleverness" component of density improvement, Moore saw a limit. Although improvements in device isolation and the development of the MOS transistor had contributed to greater packing density, Moore saw the latest circuits as near their design limits. Predicting an end to the design cleverness trend in four or five years, Moore predicted a change in the slope of his trend from doubling every year, to doubling every two years (Figure 2).

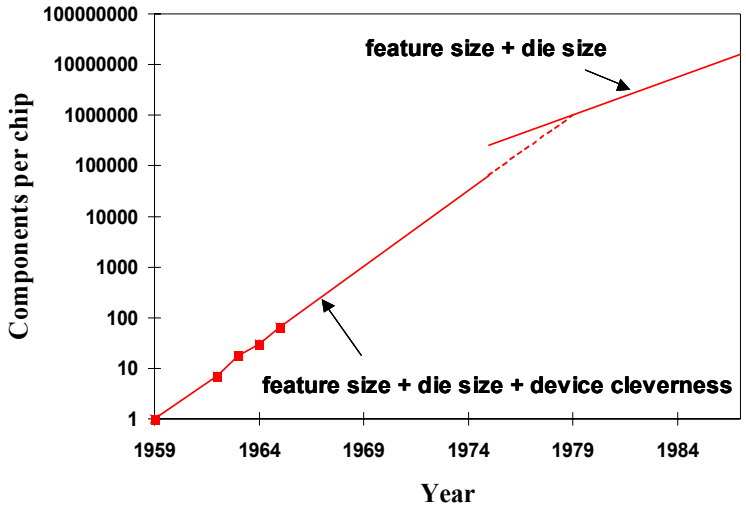


Figure 2. Moore's second observation of 1975 showing his prediction of a change in slope, from doubling the number of components each year to doubling each two years.

Moore's prediction of a slowdown was both too pessimistic and too generous. The slowdown from doubling each year had already begun by 1975 with Intel's 16Kb memory chip. The 64Kb DRAM chip, which should have been introduced in 1976 according to the original trend, was not available commercially until 1979 [3]. However, Moore's prediction of a slowdown to doubling components every two years instead of every year was too pessimistic. The 50% improvement in circuit density each year due to feature size and die size was really closer to 60% (according to Moore's retelling of the story [4]), resulting in a doubling of transistor counts per chip every eighteen months or so. Offsetting the curve to switch from component counts to transistor counts and beginning with the 64Kb DRAM in 1979, the industry followed the "new" Moore's Law trend throughout the 1980s and early 1990s.

After nearly forty years, extrapolation of Moore's Law now seems less risky. In fact, predictions of future industry performance have reached such a level of acceptance that they have been codified in an industry-sanctioned "roadmap" of the future. The *National Technology Roadmap for Semiconductors* (NTRS) [5] was first developed by the Semiconductor Industry Association in 1994 to serve as an industry standard Moore's Law. It extrapolated then current trends to the year 2010, where 70 nm minimum feature sizes were predicted to enable 64Gb DRAM chip production. This official industry roadmap has been updated many times, going international in 1999 to become the ITRS, the *International Technology Roadmap for Semiconductors*.

What is the future of Moore's Law? Recent industry trends certainly do not show a slowdown – many observers talk about an acceleration in Moore's Law. Will Moore's Law continue for the 15 years extrapolated out in the last edition of the ITRS? To answer this question, a more careful look at the drivers of Moore's Law is required.

III. Why Does Moore's Law Work?

Through a period of over 40 years the miraculous exponential growth of Moore's Law has continued. This unprecedented technological evolution begs for an explanation. Some have argued that industry momentum simply pushes semiconductor technology forward. Others describe semiconductor technology development as "fashionable" engineering, attracting the brightest minds. Most people regard Moore's Law as a self-fulfilling prophecy [6]. We all understand the economic benefits of continuing down the roadmap, and the economic consequences of falling behind our competitors. We make Moore's Law happen because we want it to be true.

Ray Kurzweil proffered a more fundamental relationship between Moore's Law and the human need to innovate [7]. Following Kurzweil's lead, let's extrapolate Moore's Law not into the future, but into the past. As Gordon Moore first described it, what has become Moore's Law began in 1959 with the manufacture of the first planar transistor. But if one expands the definition of Moore's Law and considers the longer term shrinking of electronics and electrical technology, it is possible to see that some version of Moore's Law has been going on for over one hundred years (and, interestingly, predates the birth of Gordon Moore!). Extending the feature size trend described above back into the past, Table 1 shows the retroactive Moore's Law and the electrical technology that fits the trend.

It seems that innovation has pushed electronic technology to greater miniaturization for over 100 years, making Moore's Law, or some equivalent evolutionary trend, more than just a semiconductor industry phenomenon. Surely some fundamental driver of innovation is at work here. But let's be honest –the data in Table 1 is contrived. Backtracking the Moore's Law numbers and finding some convincing technologies that fit each "node" was easy, and almost without meaning. Of course, innovation is fundamental to the human

condition, but the pace of innovation is not. One must look a little more carefully to find out how the semiconductor industry in particular has kept such a consistent pace of technology development.

Year	Feature Size	Technology
1900	1 inch	Telegraph wires
1912	1/4 inch	Electromechanical relays
1924	1/16 inch	de Forest Audion
1936	16 mils	Triode vacuum tubes
1948	4 mils	Miniature vacuum tubes
1960	1 mil (25 μm)	Planar transistor

Table 1. A retroactive look at Moore's Law.

Ultimately, the drivers for technology development fall into two categories: push and pull. Push drivers are technology enablers, those things that make it possible to achieve the technical improvements. Moore described the three push drivers as increasing chip area, decreasing feature size, and design cleverness. Pull drivers are the economic drivers, those things that make it worth while to pursue the technical innovations. Although, as we shall see, the two drivers are not independent, it is the econmic drivers that always dominate. As Bob Noyce, cofounder of Intel, wrote in 1977 [8] "…further miniaturization is less likely to be limited by the laws of physics than by the laws of economics."

The economic drivers for Moore's Law are extraordinarily compelling. As the dimensions of a transistor shrink, the transistor becomes smaller, lighter, faster, consumes less power, and in many cases is more reliable. All of these factors make the transistor more desirable for virtually every possible application. But there is more. Historically, the semiconductor industry has been able to manufacture silicon devices at an essentially constant cost per area of processed silicon. Thus, as the devices shrink they enjoy a shrinking cost per transistor. As many have observed, it is a life without tradeoffs (unless, of course, you consider the stress on the poor engineers trying to make all of this happen again and again). Each step along the roadmap of Moore's Law virtually guarantees economic success.

It is interesting to note that the most compelling benefits of Moore's Law, a better transistor at a lower cost, does not fundamentally rely on increasing the number of transistors per chip. Certainly the increased memory capacity and/or functional abilities of more complex chips enable new applications that increase the demand for chips. But this high end driver does not account for the majority of chips produced. The ability to produce moderate functionality at incredibly low prices enables new mass markets (like the microprocessor running Linux in my microwave oven, or that fact that my dishwasher has more compute power than existed in the world in 1950). For these applications, increased functions per chip is not important. Increased circuit density, which drives down costs and improves chip performance, is an enabler for all applications.

IV. Redefining Moore's Law

The economic realities of increased circuit density and other market trends have conspired to redefine Moore's Law. A look at the trend of DRAM chip deliveries in the last five years shows a remarkable change – the number of transistors per chip has not been growing at anywhere near the historical pace of the past few decades. Examining the number of transistors used by each microprocessor generation also shows that the historical Moore's Law, doubling the number of transistors each 18 months, has not been matched in

microprocessor manufacture for some time [3]. Simply put, the capability to make a large number of transistors on a chip has outstrip the market demand for those chips. Why aren't 4Gb DRAM chips in mass production today, as the historical Moore's Law trend would suggest? Quite simply, there is no mass market demand for such a chip. Why don't microprocessors use as many transistors as our manufacturing capabilities would allow? Because the microprocessor designers (the customers of those transistors) can't yet design a chip to use that many transistors.

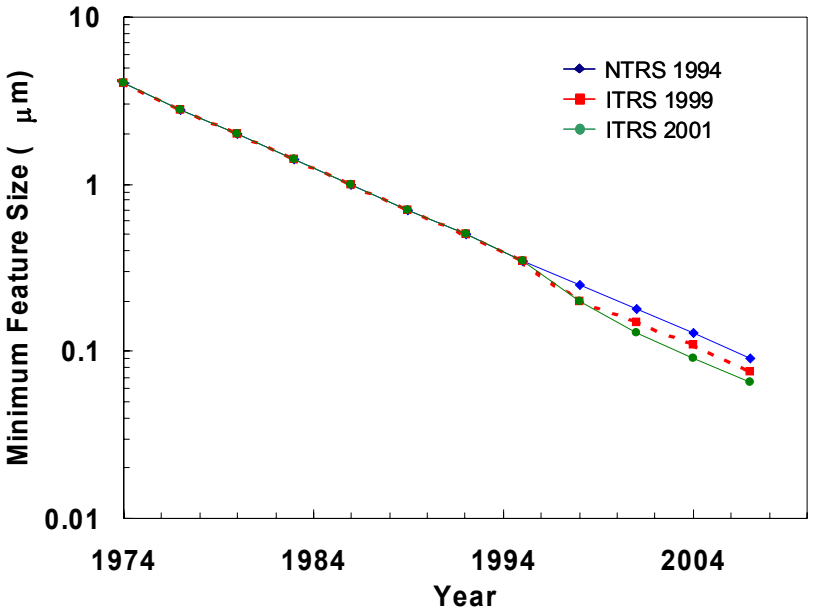
So is Moore's Law dead? Not at all. The greatest value of Moore's Law comes from improved circuit density and transistor performance, not increased functions per chip. Moore's Law is not about scaling up, it is about scaling down. It is the shrinking transistor that creates the compelling economic advantages of Moore's Law. As long as transistor scaling continues, Moore's Law remains alive and well. In fact, this realization is implicitly coded into the latest editions of the ITRS. While the first NTRS named each technology "node" or generation after the DRAM generation that it enabled (e.g., the 64Mb node), recent roadmaps simply label the nodes by their lithographic feature size (the 130nm node, for example, is currently ramping into mass production). Transistor scaling continues, and is now the only true measure of Moore's Law.

V. Moore's Law as a Learning Curve

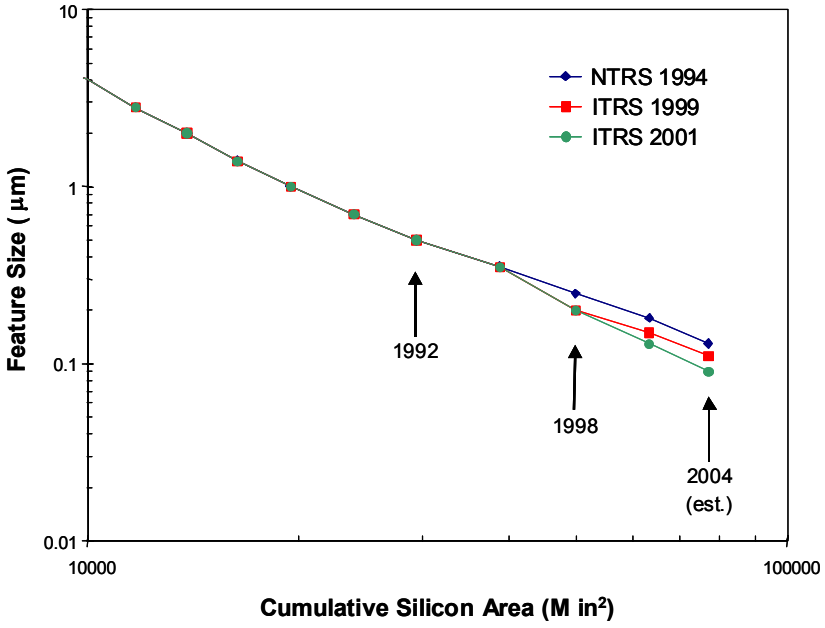
The economic drivers for Moore's Law are clear and compelling. They explain why Moore's Law exists. But they don't explain how. One possible explanation comes from learning curve theory. The basic tenet of learning curve theory is that a consistent improvement in performance of some task is possible through increasing practice. To be specific, the "learning curve" expresses a constant percent improvement in some performance metric each time the cumulative number of trials, or practice attempts, is doubled. By plotting the performance metric of interest as a function of the cumulative output of a person, factory, or industry, learning curve theory predicts a straight line on a log-log scale.

How can learning curves be applied to the semiconductor industry? The discussion above makes it clear that the metric of interest is the transistor size. But what is the measure of "practice", the cumulative output of the industry? One thing is certain, time should not be used as the independent variable. Although there can be some debate, I propose cumulative area of silicon produced by the industry as the most appropriate metric of industry output. Figure 3 shows this new formulation of Moore's Law as a learning curve, compared to the traditional time-based expression.

Looking at the historical trend shown in Figure 3b, there is a roughly linear progression (on the log-log scale, of course) of minimum feature size as a function of cumulative area of silicon produced by the industry. There is a distinct slowdown of the learning curve in the 1990 – 1995 timeframe, speeding back up to the historical trend by 1996 – 1998. It is interesting to contrast this observation based on the learning curve version of Moore's Law with the traditional view. As Figure 3a shows, the time-based view of Moore's Law saw no slowdown in the early 1990s, and has shown an acceleration of Moore's Law over the last 6 years or so. Note that changed predictions of Moore's Law found in the 1994 through 2001 roadmaps, while often called an "acceleration" of Moore's Law, can be seen in the learning curve formulation as a correction back to the historical trend line from the slowdown of the early 1990s.



(a)



(b)

Figure 3. Moore's Law shown (a) as the traditional time-based progression, and (b) as a learning curve, plotting minimum feature size versus cumulative area of silicon produced by the industry on a log-log scale.

What is the advantage of using this new learning curve formulation of Moore's Law? If the trends in our industry can in fact be explained by learning curve theory, one would expect this new formulation to be more predictive of future trends. Given a prediction of when silicon output of the industry would grow to a given level, one could predict, through an extrapolation of Figure 3b, what lithographic feature size would be available at that time. But besides the hope for quantitative predictability based on Moore's learning law, this formulation makes it perfectly clear that silicon volume drives continued innovation. In order to continue Moore's Law, an ever increasing output of silicon is required.

VI. Coupling Technology to Economics – the Limits of Moore's Law

The discussion above emphasizes the important role of economics in Moore's Law. But surely continuation of the IC evolution to allow smaller and smaller features is dependent on technology development, not just economics? Of course. There is a critical technology/economy cycle that roles down the slope of Moore's Law. A technological development that enables the cost effective manufacture of smaller transistors allows the manufacturer to offer a new desirable product to the market place (faster, smaller, cheaper). This new capability (either due to an increase in performance or a decrease in cost, or both) creates a new market for the product, which increases the volume of sales. Higher sales volumes allow a percentage of those sales to be reinvested in the development of the next technology evolution (the cause and effect relationship of an industry learning curve). Even though each technology generation requires an increasing investment for development, the higher sales volume driven by the newly enabled markets justifies the investment. Technology development feeds economic growth which allows investment in further technology development.

But, as Gordon Moore himself has said many times, no exponential is forever. There are both economic limits and technology limits (no amount of money can be used to overcome the laws of physics). The economic limits are defined by the growing demand for more silicon. If demand growth slows, so will Moore's Law. On the technology side, increasingly costly manufacturing processes required by the smaller transistors may cause an increase in the historical manufacturing cost per area of silicon. Higher cost per function limits the potential for growth of new markets, which lowers the growth of cumulative silicon area, which slows the learning.

Using optical lithography as an example, current manufacturing techniques push the absolute physical limits of what is possible to achieve. As we approach the "brick wall" physical limits of the imaging technology, the cost required to get an incremental improvement in performance rises exponentially [9]. And, as illustrated in Figure 4a, the economic limit is always reached before the physical limit. Fortunately, the picture depicted in Figure 4a is rarely a static one. Innovation can move the brick wall (which is sometimes a perceived limit rather than an actual one), allowing us to jump to a more beneficial capability versus cost curve. In optical lithography, the combination of phase shifting masks, off-axis illumination, and optical proximity correction have moved the brick wall of ultimate resolution lower by a factor of two. Note that the new cost/capability curve is initially higher cost for a given capability than the previous curve. But as the capability required for manufacturing is raised, a cross-over point is reached where the new technology is more cost effective than trying to push the old technology closer to its limit. At this point, the wise lithographer makes the leap to the new innovation.

Each generation of process technology developed to enable one more node on the ITRS roadmap requires a host of new and expensive equipment and materials. In what has sometimes been called Moore's second law, the cost of new fabrication facilities seems to rise exponentially over time. And yet the economic driver of Moore's Law requires significant reductions in the cost per transistor over time. In fact, the amazing economic reality of the semiconductor industry is that the cost of producing one square

centimeter of finished silicon has remained approximately constant (or has risen only slowly) throughout the entire history of the semiconductor industry. How has this been accomplished?

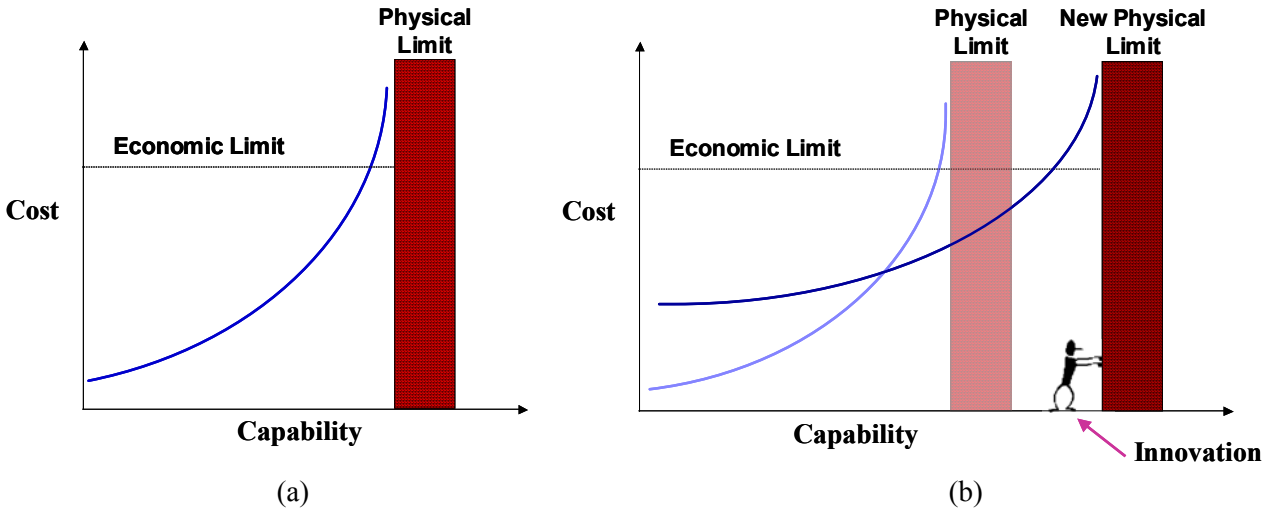


Figure 4. The relationship between capability and cost for (a) a given technology as the physical limits of that technology are approached, and (b) the role of innovation in changing the physical limits, and thus the cost/capability curve.

There have been three main avenues to control manufacturing costs per area of silicon in the presence of dramatically rising equipment and material costs: increasing wafer sizes, increasing yields, and improved equipment effectiveness. From the one inch wafers used 40 years ago to the 300mm (12 inch) wafers becoming popular today, this increase in wafer size takes advantage of the fact that some processing costs are essentially per wafer rather than per unit area. Thus, an increase in wafer size can actually reduce the processing costs per unit area of silicon. As the slow transition of the industry to 300mm wafers has shown, however, there is no guarantee that larger wafers will be more cost effective and significant development effort is required to provide improved process quality over larger wafer sizes at reduced cost per unit area. It is unclear whether wafers larger than 300mm will prove cost effective.

The second method for improving device costs is to improve the yield of the devices. In essence, it costs about the same to build a non-working device as it does to build a working device. Thus, all other things being equal, a process with 50% yield will have twice the cost per finished, saleable device than a process with 100% yield. In the 1970s, yields of 20 – 40% for leading edge products were not uncommon. By the 1980s, 50 – 70% yields were the norm. By the 1990s chip makers came to expect 80 – 90% yields during volume production. While this trend has resulted in considerable cost improvements for the industry, there is little upside left with respect to yield. The emphasis today is on increasing the ramp to high yield, that is, decreasing the time from first silicon to 90%+ yield so that the average fab throughput of good devices is nearer its theoretical maximum.

Overall equipment effectiveness is the final, and possibly most significant, enabler for low cost semiconductor manufacturing. By far the most important component of equipment effectiveness is throughput. Taking lithography exposure tools as an example, a stepper in 1980 costs $500K, while a scanner today may run over $10M. However, that 1980 stepper had a maximum throughput of 40 four inch wafers per hour, while today's scanner is capable of processing 90 300mm wafers in an hour. The result is a

roughly constant equipment cost per square centimeter of processed silicon. There is still room for improvement. Fabs typically average actual throughputs in the lithography bay that are less than half of the theoretical maximum.

VII. Innovations in Lithography

By redefining Moore's Law as a transistor density trend, the minimum lithographic feature size takes on the dominant role as the industry's technology metric. Of course, many other important factors such as overlay capability, gate oxide thickness, junction depth, etc., must scale with minimum feature size in order to gain the benefits of the transistor shrink. While each of these factors represents great technical challenges, cost effective lithography has traditionally been the limiter in the progress of Moore's Law. Over the years many innovations in optical lithography have moved the physicals limits and kept the costs acceptable for ever improving capabilities. These innovations have included

- Wavelength reduction
- Increasing numerical apertures
- Resolution enhancement technologies
- Improved resist performance
- Reduced process variations
- Advanced process control

More innovations are still possible, such as

- Wavelength reduction to 157nm
- Increased numerical apertures to 0.9
- Immersion lithography
- Real equipment productivity that approaches the theoretical
- Improved process control
- More extensive use of phase shift masks and other "hard" resolution enhancements
- Polarization control
- Promulgation of lithography friendly designs

Through the use of innovations like those listed above, optical lithography can continue to meet the needs of the industry for the foreseeable future. However, merely developing capabilities is not enough. These capabilities must enable the required lithographic performance at the required price point.

II. Conclusions

Moore's Law is a direct consequence of the incredible and unique scaling laws of semiconductor devices. By making a transistor smaller that device becomes better in every respect: smaller, lighter, faster, lower power and cheaper. It also becomes more difficult to make, and that means the last metric, a smaller device is cheaper to make, is only true as a result of a concerted engineering effort to make it so. Moore's Law is not a law, it is an act of will. Considerable effort is devoted to its continuation because there is a strong economic incentive to do so.

The economic benefits of Moore's Law come from the shrinking of the transistor. That is why Moore's Law has drifted from its historical origins as describing the number of transistors per chip to the more important metric of minimum lithographic feature size (where a proper choice of feature is made in order to properly represent the scaling potential of the transistor). While the popular press has failed to notice this

shift, in the semiconductor industry there is no doubt that the technology nodes of Moore's Law are governed by the historical 0.7X shrink in minimum feature size per generation.

It is my opinion that Moore's Law is an example of an industry wide learning curve. There is a constant fractional improvement in technical capability (as judged by the minimum feature size, for example) for every constant fractional increase in cumulative investment of effort. Since investment effort is generally proportional to output, Moore's Law can be formulated as a learning curve by plotting minimum feature size as a function of cumulative area of silicon produced by the industry on a log-log scale. (Alternatively, total cumulative revenue of the industry can be used as the x-axis as well with virtually no change in the curve). As presented here, Moore's Law has kept on a relatively constant learning curve throughout the history of the industry, with the exception of a slowdown in the early 1990s (it would be very interesting to speculate why this slowdown occurred). Current trends are on pace with historical learning rates. With this new formulation of Moore's Law, more accurate forecasting should be possible.

The economics drivers of Moore's Law can be divided into push drivers and pull drivers. Push drivers are the technology innovations that enable low cost manufacturing of smaller transistors. Pull drivers are the new applications that these smaller, faster, cheaper, more powerful devices enable. As the discussion of Moore's Law as a learning curve should indicate, the importance of pull drivers is in the creation of increasing demand and thus increasing volume of silicon area. These two drivers, push and pull, are inexorably linked due to the relationship between capability and cost for the technology push, and the relationship between cost and demand for the volume pull. Any reduction in the force of the push or the pull drivers will result in a slowdown in the time-based Moore's Law.

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